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NTE4555B & NTE4556B
Integrated Circuit
CMOS, Dual Binary to 1–Of–4 Decoder/Demultiplexer

Description:

The NTE4555B (Active High Outputs) and NTE4556B (Active Low Outputs) are dual binary to 1–of–4 decoder/demultiplexers in a 16–Lead DIP type package constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input €, and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The NTE4555B has the selected output go to the “high” state, and the NTE4556B has the selected output go to the “low” state. Expanded decoding such as binary–to–hexadecimal (1–of–16), etc., can be achieved by using other NTE4555B or NTE4556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital date transmission systems.

Features:

- Diode Protection on All Inputs
- Noise Immunity – 45% of V_{DD} (Typ)
- Active High of Active Low Outputs
- Low Quiescent Current – 5.0nA/Package (Typ) at 5Vdc
- Expandable
- Supply Voltage Range = 3Vdc to 10Vdc
- All Outputs Buffered
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. This device contains circuitry to protect the input against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current	I_{OH}									
(V_{OH} = 2.5Vdc) Source		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	mAdc
(V_{OH} = 4.6Vdc)			−0.25	–	−0.2	−0.36	–	−0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	mAdc
(V_{OL} = 0.4Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance, Pin2 or Pin14	C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	15	–	0.015	15	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 5)	I_T	5	$I_T = (0.85\mu A/kHz)\ f + I_{DD}$							µAdc
		10	$I_T = (1.7\mu A/kHz)\ f + I_{DD}$							µAdc
		15	$I_T = (2.6\mu A/kHz)\ f + I_{DD}$							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (3.0ns/pf) C_L + 30ns	t_{TLH}	5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time t_{THL} = (1.5ns/pf) C_L + 25ns	t_{THL}	5.0	–	100	200	ns
t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, A, B to Output t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 135ns	t_{PLH}, t_{PHL}	5.0	–	220	440	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 62ns		10	–	95	190	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 45ns		15	–	70	140	ns
Propagation Delay Time, E to Output t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 115ns	t_{PLH}, t_{PHL}	5.0	–	200	400	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 52ns		10	–	85	170	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 40ns		15	–	65	130	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

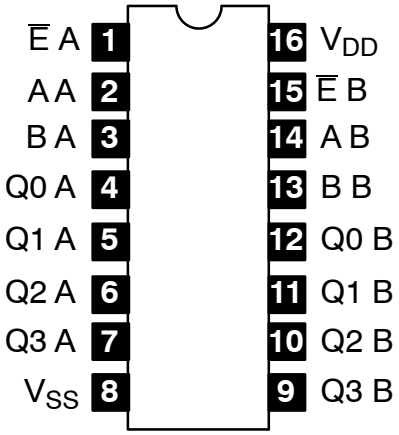
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

Inputs			Outputs NTE4555B				Outputs NTE4556B			
Enable	Select									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	$\overline{Q}$3	$\overline{Q}$2	$\overline{Q}$1	$\overline{Q}$0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don’t Care

Pin Connection Diagram



NTE4555B: Output “High” on Select
NTE4556B: Output “Low” on Select