ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4531B & NTE4531BT
Integrated Circuit
CMOS, 12–Bit Parity Tree

Description:

The NTE4531B (16–Lead DIP) and NTE4531BT (SOIC–16) are 12–bit parity tree devices constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data–bit inputs (D0 thru D11), an even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12–bits can be accommodated by cascading other NTE4531B devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

Features:

- Noise Immunity = 45% of V_{DD} (Typ)
- Supply Voltage Range: 3Vdc to 18Vdc
- All Output Buffered
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Quiescent Current = 5nA/Package (Typ) at 5Vdc
- Variable Word Length
- Diode Protection on All Inputs

Absolute Maximum Ratings: (Voltages referenced to V_{SS})

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Electrical Characteristics: (Note 1)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 3) “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 123.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current	I_T	5.0	I_T = (0.25µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 2, Note 4)		10	I_T = (0.50µA/kHz) f + I_{DD}							µAdc
		15	I_T = (0.75µA/kHz) f + I_{DD}							µAdc

Note 1. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 2. The formulas given are for the typical characteristics only at +25°C.

Note 3. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 1)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, Data to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 355ns		5.0	–	440	1320	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 142ns		10	–	175	525	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 95ns		15	–	120	360	ns
Propagation Delay Time, Odd/Even to Q	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 165ns		5.0	–	250	750	
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 67ns		10	–	100	300	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 45ns		15	–	70	210	ns

Note 1. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 2. The formulas given are for the typical characteristics only at +25°C.

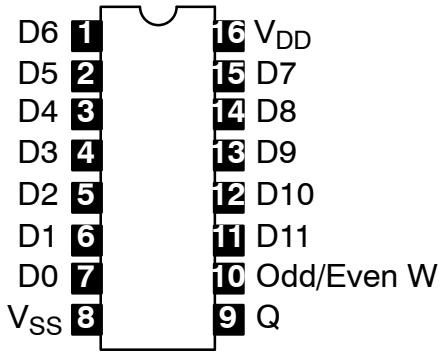
Truth Table

Inputs								Output
W	D11	D10	• • •	D2	D1	D0	Decimal (Octal) Equivalent	Q *
0	0	0	• • •	0	0	0	0 (0)	0
0	0	0	• • •	0	0	1	1 (1)	1
0	0	0	• • •	0	1	0	2 (2)	1
0	0	0	• • •	0	1	1	3 (3)	0
0	0	0	• • •	1	0	0	4 (4)	1
0	0	0	• • •	1	0	1	5 (5)	0
0	0	0	• • •	1	1	0	6 (6)	0
0	0	0	• • •	1	1	1	7 (7)	1
•	•	•		•	•	•	•	•
•	•	•	• • •	•	•	•	•	•
•	•	•		•	•	•	•	•
1	1	1	• • •	0	0	0	8184 (177770)	0
1	1	1	• • •	0	0	1	8185 (177771)	1
1	1	1	• • •	0	1	0	8186 (177772)	1
1	1	1	• • •	0	1	1	8187 (177773)	0
1	1	1	• • •	1	0	0	8188 (177774)	1
1	1	1	• • •	1	0	1	8189 (177775)	0
1	1	1	• • •	1	1	0	8190 (177776)	0
1	1	1	• • •	1	1	1	8191 (177777)	1

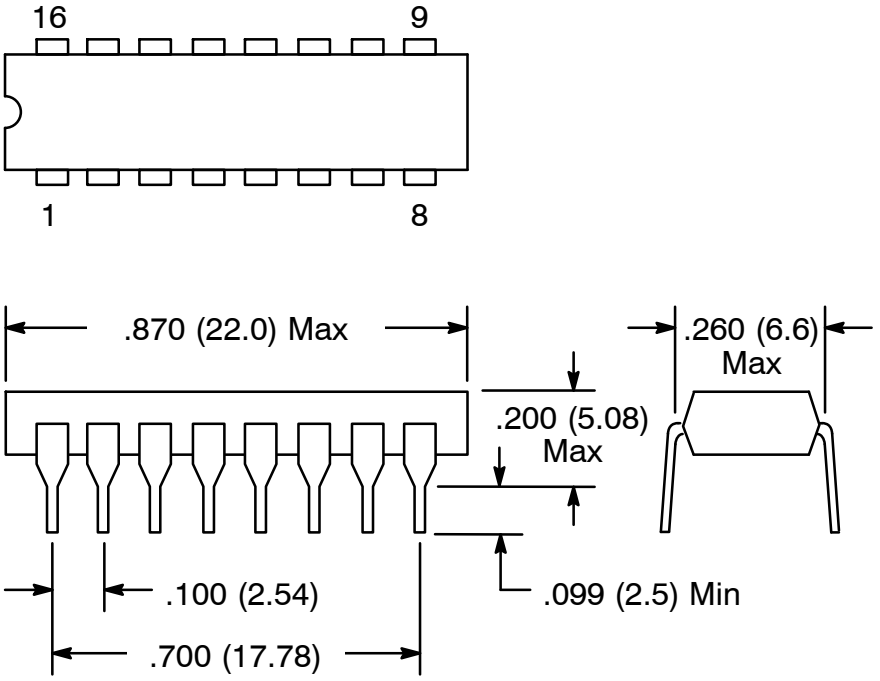
* 0 = Ever Parity, 1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D’s.

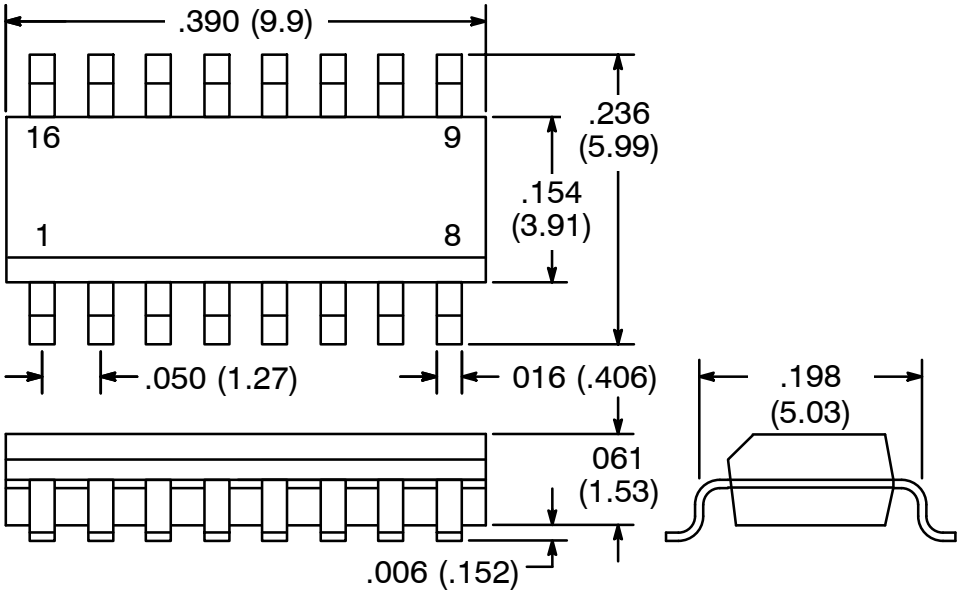
Pin Connection Diagram



NTE4531B



NTE4531BT



NOTE: Pin1 on Beveled Edge