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NTE4520B & NTE4520BT
Integrated Circuit
CMOS, Dual Binary Up Counter Counter

Description:

The NTE4520B (16–Lead DIP) and NTE4520BT (SOIC–16) are dual binary up counters constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4–stage counters. The counter stages are type D flip–flops, with interchangeable Clock and Enable lines for incrementing on either the positive–going or negative–going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line.

These complementary MOS up counters find primary use in multi–stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

Features:

- Quiescent Current = 5nA/Package (Typ) at 5Vdc
- Noise Immunity = 45% of V_{DD} (Typ)
- Diode Protection on All Inputs
- Supply Voltage Range = 3Vdc to 18Vdc
- Low Input Capacitance = 5pF (Typ)
- Internally Synchronous for High Internal and External Speeds
- Logic Edge–Clocked Design – Incremental on Positive Transition of Clock or Negative Transition Enable
- 6Mhz Counting Rate
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	15	–	0.015	15	–	600	µAdc
Total Supply Current	I_T	5.0	I_T = (0.6µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on All Outputs, All Buffers Switching Note 3, Note 5)		10	I_T = (1.2µA/kHz) f + I_{DD}							µAdc
		15	I_T = (1.7µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 2 \times 10^{-3}(C_L - 50)\, V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH},					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}. t_{PHL}					
Clock to Q / Enable to Q						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 215ns		5.0	–	280	560	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 97ns		10	–	115	230	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 75ns		15	–	80	160	ns
Reset to Q						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 265ns		5.0	–	330	650	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 117ns		10	–	130	230	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 95ns		15	–	90	170	ns
Clock Pulse Width	t_{WH}, t_{WL}	5.0	200	100	–	ns
		10	100	50	–	ns
		15	70	35	–	ns
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.5	MHz
		10	–	6.0	3.0	MHz
		15	–	8.0	4.0	MHz
Clock or Enable Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	15	µs
		15	–	–	15	µs
Enable Pulse Width	$T_{WH(E)}$	5.0	440	220	–	ns
		10	200	100	–	ns
		15	140	70	–	ns
Reset Pulse Width	$T_{WH(R)}$	5.0	250	125	–	ns
		10	110	55	–	ns
		15	80	40	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

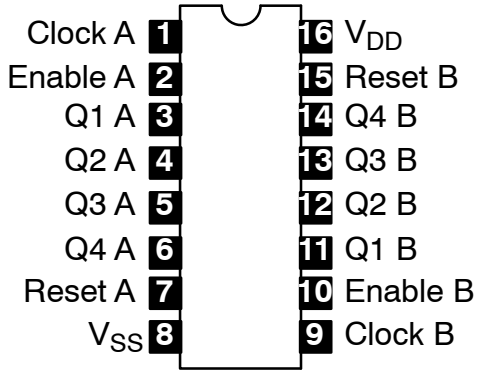
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table:

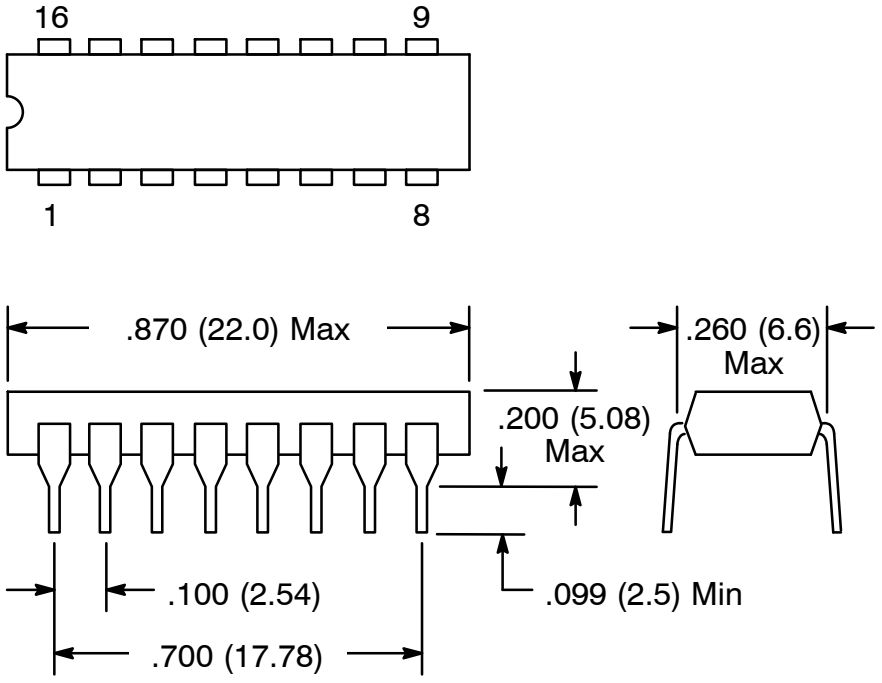
Clock	Enable	Reset	Action
⎍	1	0	Increment Counter
0	⎎	0	Increment Counter
⎎	X	0	No Change
X	⎍	0	No Change
⎍	0	0	No Change
1	⎎	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don’t Care

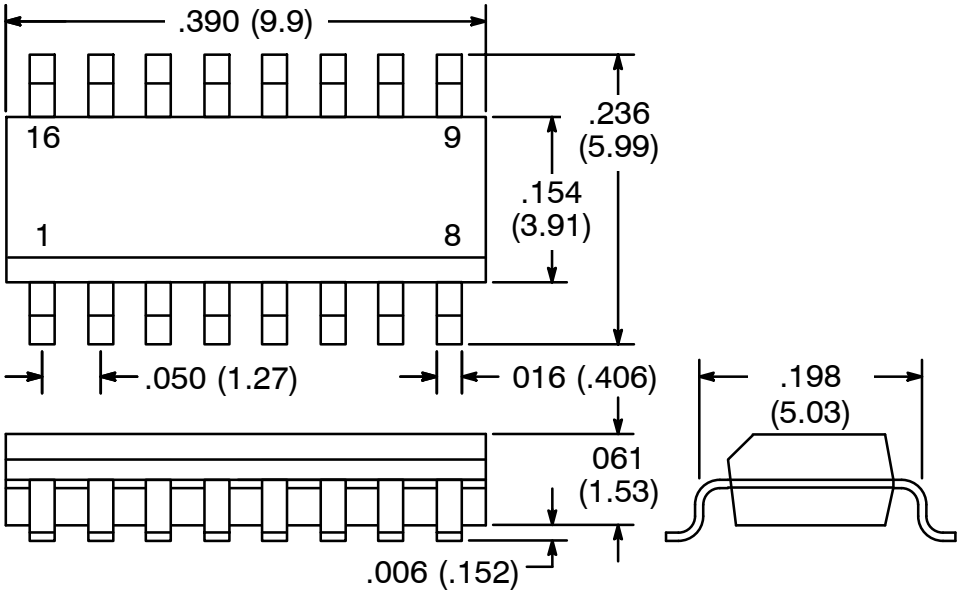
Pin Connection Diagram



NTE4520B



NTE4520BT



NOTE: Pin1 on Beveled Edge