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# NTE4076B
# Integrated Circuit
# CMOS, 4–Bit D–Type Register with Three–State Outputs

**Description:**

The NTE4076B is a 4–Bit Register in a 16–Lead DIP type package consisting of four D–type flip–flops operating synchronously from a common clock. OR gated output–disable inputs force the outputs into a high–impedance state for use in bus organized systems. OR gated data–disable inputs cause the Q outputs to be fed back to the D inputs of the flip–flops. Thus, they ar inhibited from hanging state while the clocking process remains undisturbed. An asynchronous master reset is provided to clear all four flip–flops simultaneously independent of the clock or disable inputs.

**Features:**

- Three–State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Quiescent Current = 0.5nA Typ/Pkg at 5 Vdc
- Supply Voltage Range = 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

**Absolute Maximum Ratings:** (Voltages Referenced to $V_{SS}$, Note 1)

DC Supply Voltage, $V_{DD}$ . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), $V_{in}$ . . . . . –0.5 to $V_{DD}$ + 0.5V
DC Current Drain (Per Pin), I . . . . . 10mA
Operating Temperature Range, $T_{sA}$ . . . . . –55 to +125°C
Storage Temperature Range, $T_{stg}$ . . . . . –65 to +150°C

Note 1. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation is is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

**Electrical Characteristics:** (Voltages referenced to $V_{SS}$, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | −55°C | | +25°C | | | +125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| Output Voltage "0" Level | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| "1" Level | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | Vdc |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | Vdc |
| Input Voltage "0" Level | $V_{IL}$ | | | | | | | | | |
| ($V_O$ = 4.5 or 0.5Vdc) | | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | Vdc |
| ($V_O$ = 9.0 or 1.0Vdc) | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | Vdc |
| ($V_O$ = 13.5 or 1.5Vdc) | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | Vdc |
| "1" Level | $V_{IH}$ | | | | | | | | | |
| ($V_O$ = 0.5 or 4.5Vdc) | | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | Vdc |
| ($V_O$ = 1.0 or 9.0Vdc) | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | Vdc |
| ($V_O$ = 1.5 or 13.5Vdc) | | 15 | 11.0 | – | 11.0 | 8.25 | – | 11.0 | – | Vdc |
| Output Drive Current Source | $I_{OH}$ | | | | | | | | | |
| ($V_{OH}$ = 2.5Vdc) | | 5.0 | –1.2 | – | –1.0 | –1.7 | – | –0.7 | – | mAdc |
| ($V_{OH}$ = 4.6Vdc) | | 5.0 | –0.25 | – | –0.2 | –0.36 | – | –0.14 | – | mAdc |
| ($V_{OH}$ = 9.5Vdc) | | 10 | –0.62 | – | –0.5 | –0.9 | – | –0.35 | – | mAdc |
| ($V_{OH}$ = 13.5Vdc) | | 15 | –1.8 | – | –1.5 | –3.5 | – | –1.1 | – | mAdc |
| Sink | $I_{OL}$ | | | | | | | | | |
| ($V_{OL}$ = 0.4Vdc) | | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5Vdc) | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | mAdc |
| ($V_{OL}$ = 1.5Vdc) | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | mAdc |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±0.1 | µAdc |
| Input Capacitance ($V_{IN}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current | $I_{DD}$ | 5.0 | – | 5.0 | – | 0.005 | 5.0 | – | 150 | µAdc |
| (Per Package) | | 10 | – | 10 | – | 0.010 | 10 | – | 300 | µAdc |
| | | 15 | – | 20 | – | 0.015 | 20 | – | 600 | µAdc |
| Total Supply Current | $I_T$ | 5.0 | $I_T$ = (0.75µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| (Dynamic plus Quiescent, Per Package, $C_L$ = 50pF on all outputs, all buffers switching, Note 3, Note 4) | | 10 | $I_T$ = (1.50µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| | | 15 | $I_T$ = (2.25µA/kHz) f + $I_{DD}$ | | | | | | | µAdc |
| Three−State Leakage Current | $I_{TL}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±3.0 | µAdc |

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 2 \times 10^{-3}(C_L - 50)\, V_{DD} f$$

where: $I_T$ is in µA (per package), $C_L$ in pF, $V_{DD}$ in volts and f in kHz is input frequency.

Note 3. The formulas given are for the typical characteristics only at +25°C.

**Switching Characteristics:** ($C_L$ = 50pF, $T_A$ = +25°C, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | | | | | |
| $t_{TLH}$ = (3.0ns/pf) $C_L$ + 30ns | | 5.0 | – | 180 | 360 | ns |
| $t_{TLH}$ = (1.5ns/pf) $C_L$ + 15ns | | 10 | – | 90 | 180 | ns |
| $t_{TLH}$ = (1.1ns/pf) $C_L$ + 10ns | | 15 | – | 65 | 130 | ns |
| Output Fall Time | $t_{THL}$ | | | | | |
| $t_{THL}$ = (1.5ns/pf) $C_L$ + 25ns | | 5.0 | – | 100 | 200 | ns |
| $t_{THL}$ = (0.75ns/pf) $C_L$ + 12.5ns | | 10 | – | 50 | 100 | ns |
| $t_{THL}$ = (0.55ns/pf) $C_L$ + 9.5ns | | 15 | – | 40 | 80 | ns |
| Propagation Delay Time | $t_{PLH}$, $t_{PHL}$ | | | | | |
| Clock to Q | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pf) $C_L$ + 215ns | | 5.0 | – | 300 | 600 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pf) $C_L$ + 92ns | | 10 | – | 125 | 250 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pf) $C_L$ + 65ns | | 15 | – | 90 | 180 | ns |
| Reset to Q | | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (1.7ns/pf) $C_L$ + 215ns | | 5.0 | – | 300 | 600 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.66ns/pf) $C_L$ + 92ns | | 10 | – | 125 | 250 | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.5ns/pf) $C_L$ + 365ns | | 15 | – | 90 | 180 | ns |
| 3−State Propagation Delay, Output “1” or “0” to High Impedance | $t_{PHZ}$, $t_{PLZ}$ | 5.0 | – | 150 | 300 | ns |
| | | 10 | – | 60 | 120 | ns |
| | | 15 | – | 45 | 90 | ns |
| 3−State Propagation Delay, High Impedance to “1” or “0” Level | $t_{PZH}$, $t_{PZL}$ | 5.0 | – | 200 | 400 | ns |
| | | 10 | – | 80 | 160 | ns |
| | | 15 | – | 60 | 120 | ns |
| Clock Pulse Width | $t_{WH}$ | 5.0 | 260 | 130 | – | ns |
| | | 10 | 110 | 55 | – | ns |
| | | 15 | 80 | 40 | – | ns |
| Reset Pulse Width | $t_{WH}$ | 5.0 | 370 | 185 | – | ns |
| | | 10 | 150 | 75 | – | ns |
| | | 15 | 110 | 55 | – | ns |
| Data Setup Time | $t_{su}$ | 5.0 | 30 | 15 | – | ns |
| | | 10 | 10 | 5 | – | ns |
| | | 15 | 4 | 2 | – | ns |
| Data Hold Time | $t_h$ | 5.0 | 130 | 65 | – | ns |
| | | 10 | 60 | 30 | – | ns |
| | | 15 | 50 | 25 | – | ns |

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

**Switching Characteristics:** ($C_L$ = 50pF, $T_A$ = +25°C, Note 2)

| Parameter | Symbol | $V_{DD}$ Vdc | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Data Disable Setup Time | $t_{su}$ | 5.0 | 220 | 110 | – | ns |
| | | 10 | 80 | 40 | – | ns |
| | | 15 | 50 | 25 | – | ns |
| Clock Pulse Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0 | – | – | 15 | μs |
| | | 10 | – | – | 15 | μs |
| | | 15 | – | – | 15 | μs |
| Clock Pulse Frequency | $f_{cl}$ | 5.0 | – | 3.6 | 1.8 | MHz |
| | | 10 | – | 9.0 | 4.5 | MHz |
| | | 15 | – | 12 | 6.0 | MHz |

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

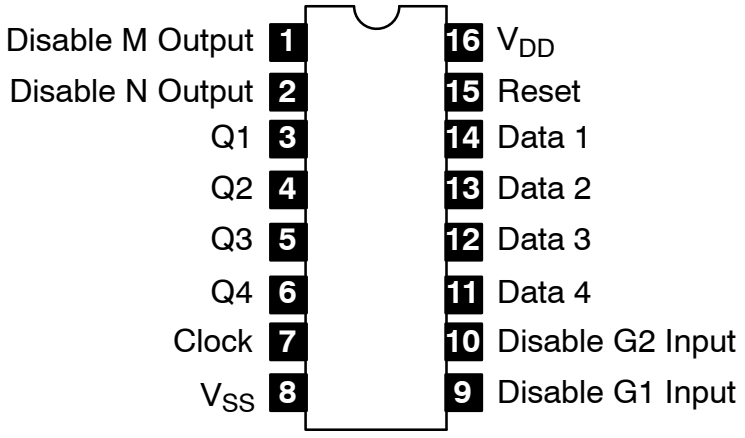
**Function Table:**

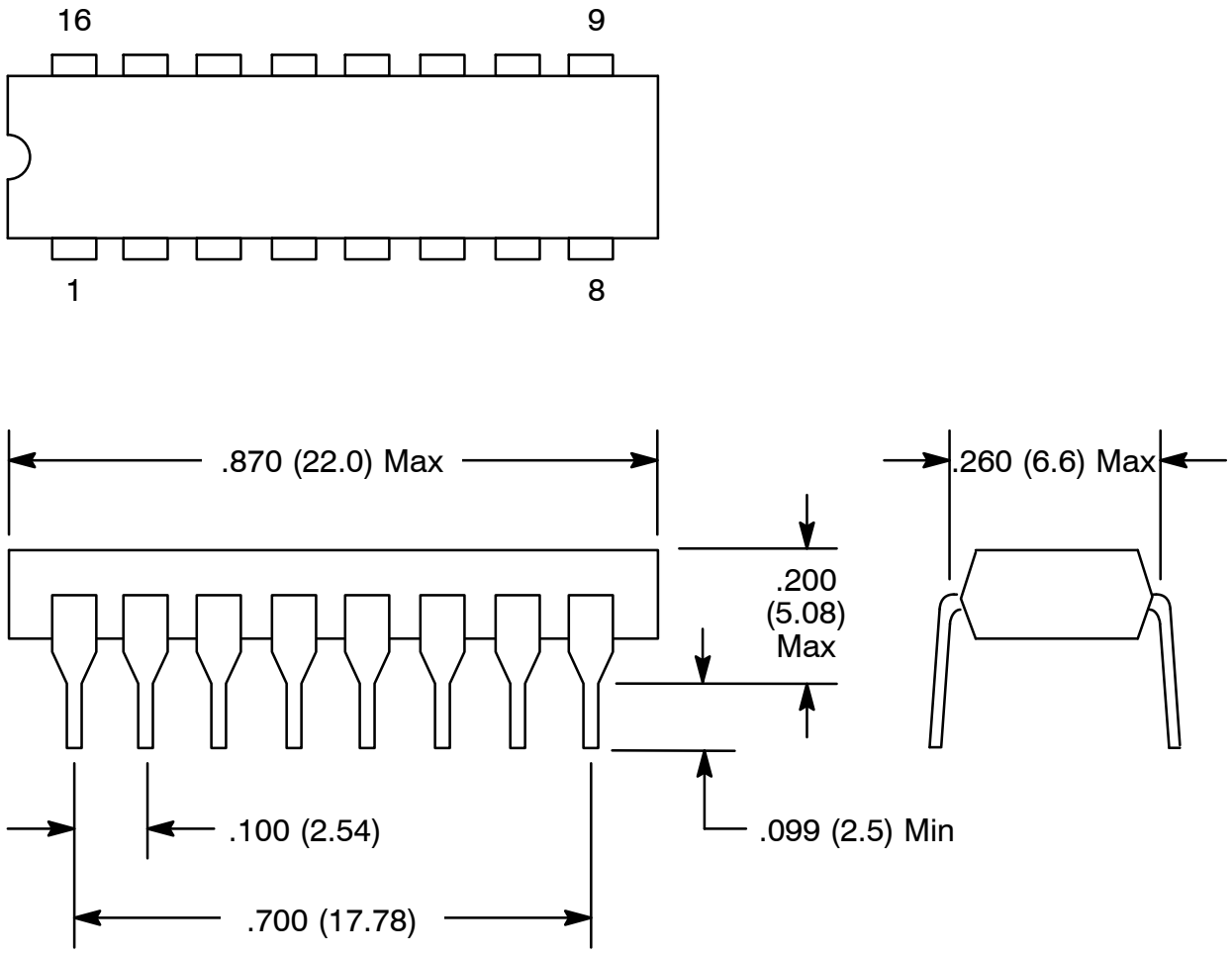
| Inputs | | | | | Output Q |
|---|---|---|---|---|---|
| | | Data Disable | | | |
| Reset | Clock | A | B | Data D | |
| 1 | X | X | X | X | 0 |
| 0 | 0 | X | X | X | $Q_n$ |
| 0 | ⎍ | 1 | X | X | $Q_n$ |
| 0 | ⎍ | X | 1 | X | $Q_n$ |
| 0 | ⎍ | 0 | 0 | 0 | 0 |
| 0 | ⎍ | 0 | 0 | 1 | 1 |

When either output disable A or B (or both) is (are) high, the output is disabled to the high impedance state; however sequential operation of the flip–flops is not affected.

X = Don’t Care

**Pin Connection Diagram**




16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)