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NTE4060B and NTE4060BT
Integrated Circuit
CMOS 14–Stage Ripple–Carry
Binary Counter/Divider and Oscillator

Description:

The NTE4052B (16–Lead DIP) and NTE4060BT (SOIC–16) are 14–stage binary ripple counters with an on–chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

Features:

- Fully static operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0V to 18V
- Capable of Driving Two Low–power TTK Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range.
- Buffered Outputs Available from Stages 4 through 10 and 12 through 14.
- Common Reset Line

Absolute Maximum Ratings: (Voltages Referenced to V_{SS})

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Stresses exceeding maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Note 2. These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g. eiher V_{SS}, V_{EE} or V_{DD}), Unused outputs must be left open.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 3)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Input Voltage "0" Level	V_{IL}									
(For Input 11 and Output 10)										
(V_O = 4.5Vdc)		5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc
(V_O = 9.0Vdc)		10	–	2.0	–	4.50	2.0	–	2.0	Vdc
(V_O = 13.5Vdc)		15	–	2.5	–	6.75	2.5	–	2.5	Vdc
"1" Level	V_{IH}									
(V_O = 0.5Vdc)		5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
(V_O = 1.0Vdc)		10	8.0	–	8.0	5.50	–	8.0	–	Vdc
(V_O = 1.5Vdc)		15	12.5	–	12.5	8.25	–	12.5	–	Vdc
Output Drive Current Source	I_{OH}									
(Except Source Pin9 and Pin10)										
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current	I_T	5.0	I_T = (0.25µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 4, Note 5)		10	I_T = (0.54µA/kHz) f + I_{DD}							µAdc
		15	I_T = (0.85µA/kHz) f + I_{DD}							µAdc

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time (Counter Outputs)	t_{TLH}	5.0	–	40	200	ns
		10	–	25	100	ns
		15	–	20	80	ns
Output Fall Time (Counter Outputs)	t_{THL}	5.0	–	50	200	ns
		10	–	30	100	ns
		15	–	20	80	ns
Propagation Delay Time Clock to Q4	t_{PLH}, t_{PHL}	5.0	–	415	740	ns
		10	–	175	300	ns
		15	–	125	200	ns
Clock to Q14		5.0	–	1.5	2.7	µs
		10	–	0.7	1.3	µs
		15	–	0.4	1.0	µs
Clock Pulse Width	t_{wH}	5.0	100	65	–	ns
		10	40	30	–	ns
		15	30	20	–	ns
Clock Pulse Frequency		5.0	–	5.0	3.5	MHz
		10	–	14	8	MHz
		15	–	17	12	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				ns
		15				ns
Reset Pulse Width	t_w	5.0	120	40	–	ns
		10	60	15	–	ns
		15	40	10	–	ns
Propagation Delay Time, Reset to On	t_{PHL}	5.0	–	170	350	ns
		10	–	80	160	ns
		15	–	60	100	ns

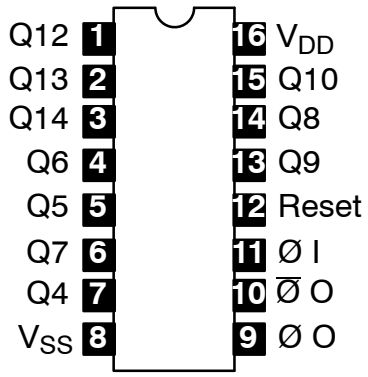
Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Truth Table:

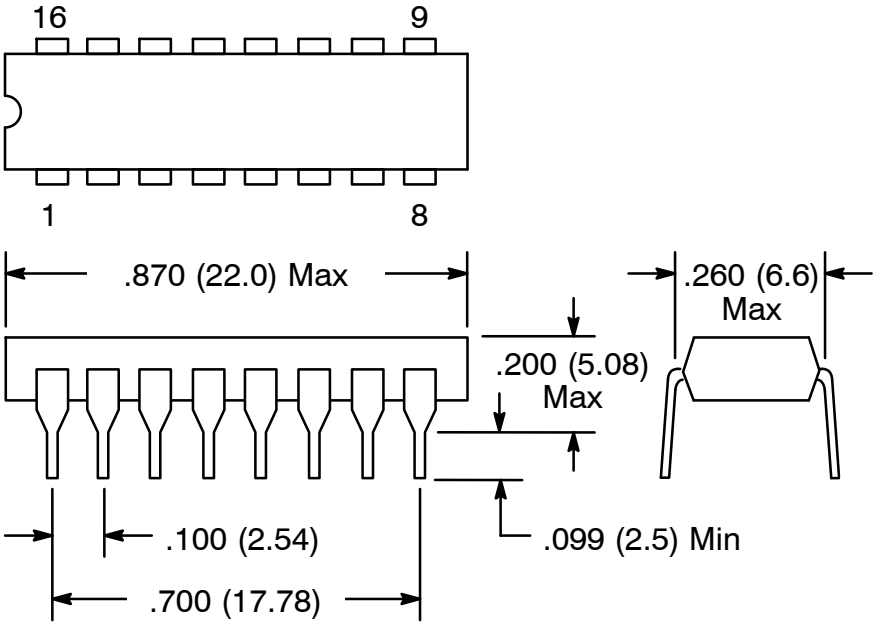
Clock	Reset	Output Stage
⎍	L	No Change
⎎	L	Advance to Next State
X	H	All Outputs are Low

X = Don’t Care

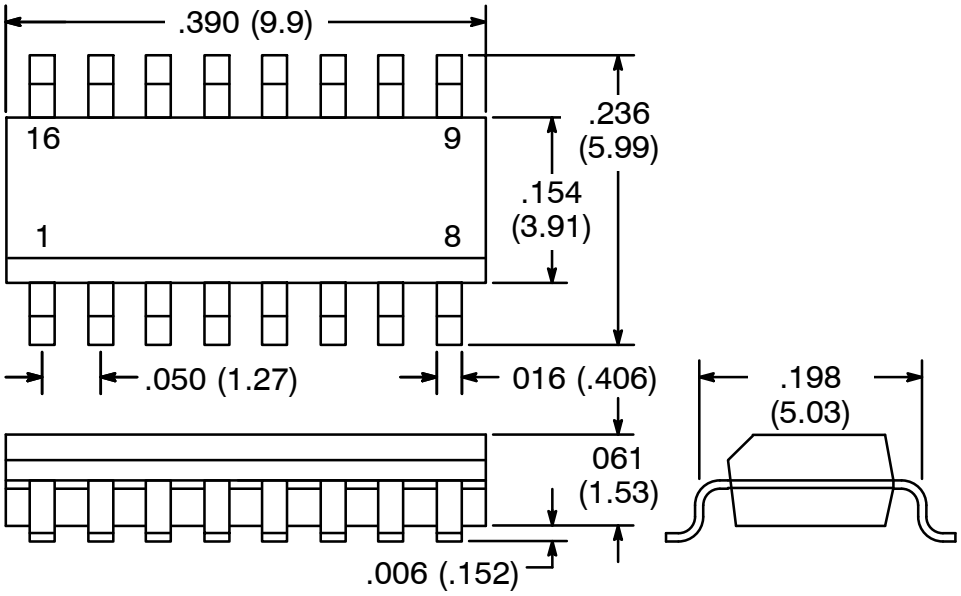
Pin Connection Diagram



NTE4060B



NTE4060BT



NOTE: Pin1 on Beveled Edge