ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4044B & NTE4044BT
Integrated Circuit
CMOS, Quad NAND R/S Latch

Description:

The NTE4044B (16–Lead DIP) and NTE4044BT (SOIC–16) are R–S latch devices constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

Features:

- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range: 3Vdc to 18Vdc

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	µAdc
		15	–	4.0	–	0.006	4.0	–	120	µAdc
Total Supply Current	I_T	5.0	I_T = (0.58µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs all buffers switching, Note 3, Note 4)		10	I_T = (1.15µA/kHz) f + I_{DD}							µAdc
		15	I_T = (1.73µA/kHz) f + I_{DD}							µAdc
Three−State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±0.1	µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{PHL} = (1.35ns/pf) C_L + 32.5ns	t_{TLH}, t_{PHL}	5.0	–	100	200	ns
t_{TLH}, t_{PHL} = (0.60ns/pf) C_L + 20ns		10	–	50	100	ns
t_{TLH}, t_{PHL} = (0.40ns/pf) C_L + 20ns		15	–	40	80	ns
Propagation Delay Time t_{PLH}, t_{PHL} = (0.90ns/pf) C_L + 130ns	t_{PLH}. t_{PHL}	5.0	–	175	350	ns
t_{PLH}, t_{PHL} = (0.36ns/pf) C_L + 57ns		10	–	75	175	ns
t_{PLH}, t_{PHL} = (0.26ns/pf) C_L + 47ns		15	–	60	120	ns
Set, $\overline{\text{Set}}$ Pulse Width	t_W	5.0	200	80	–	ns
		10	100	40	–	ns
		15	70	30	–	ns
Reset, $\overline{\text{Reset}}$ Pulse Width	t_W	5.0	200	80	–	ns
		10	100	40	–	ns
		15	70	30	–	ns
Three−State Enable/Disable Delay	t_{PLZ}. t_{PHZ}, t_{PZL}, t_{PZH}	5.0	–	150	300	ns
		10	–	80	160	ns
		15	–	55	110	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table:

Q	S	R	E
High Impedance	X	X	0
No Change	0	0	1
0	0	1	1
1	1	0	1
1	1	1	1

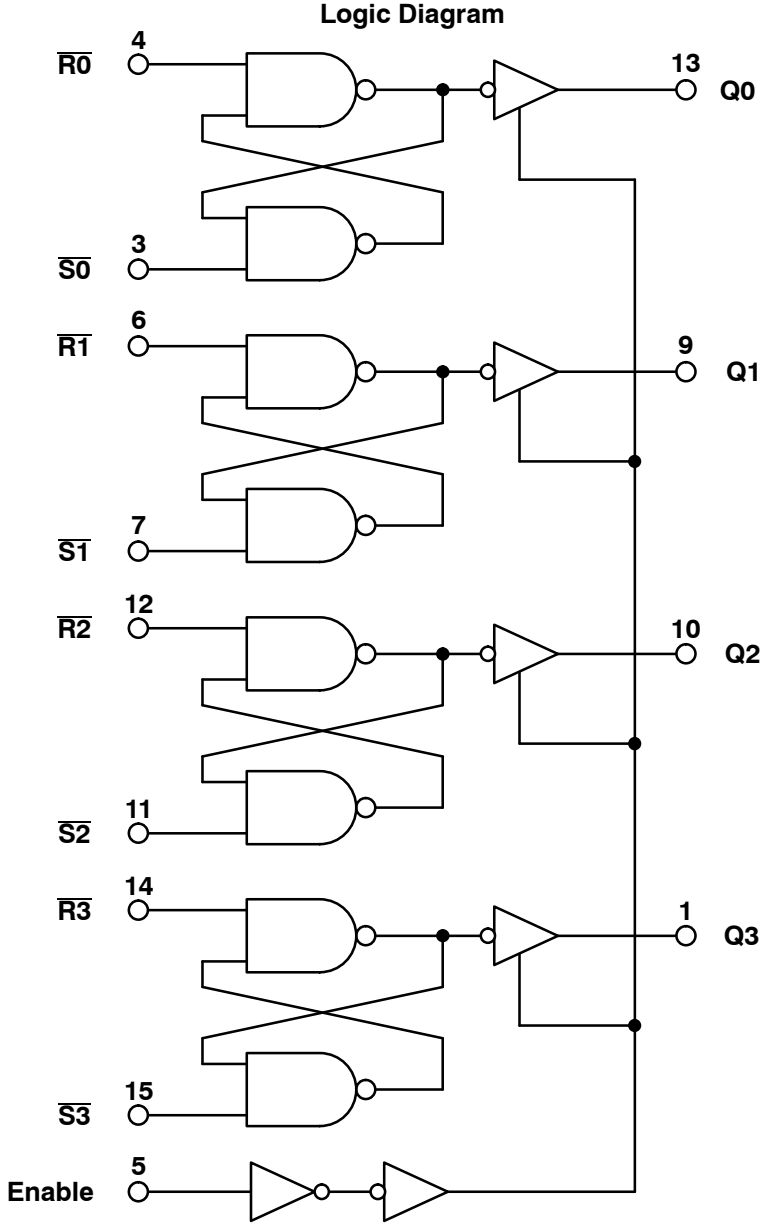
X = Don’t Care

Tthree−State Enable/Disable Delays:

Set. Reset, Enable, and Switch Conditions for 3−State Tests

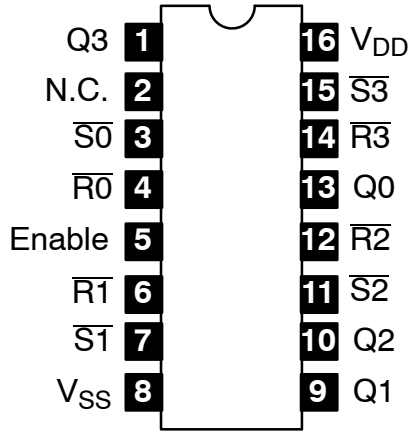
Test	Enable	S1	S2	Q	S	R
t_{PZH}	⎍	Open	Closed	A	V_{SS}	V_{DD}
t_{PZL}	⎍	Closed	Open	B	V_{DD}	V_{SS}
t_{PHZ}	⎏	Open	Closed	A	V_{SS}	V_{DD}
t_{PLZ}	⎏	Closed	Open	B	V_{DD}	V_{SS}

Logic Diagram



V_{DD} = Pin16
V_{SS} = Pin8
N.C = Pin2

Pin Connection Diagram



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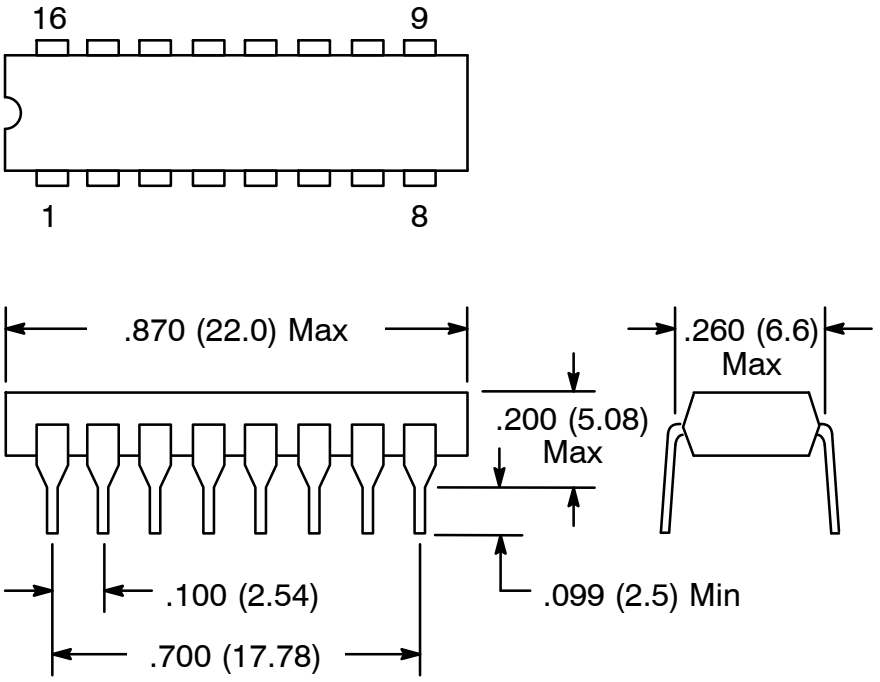
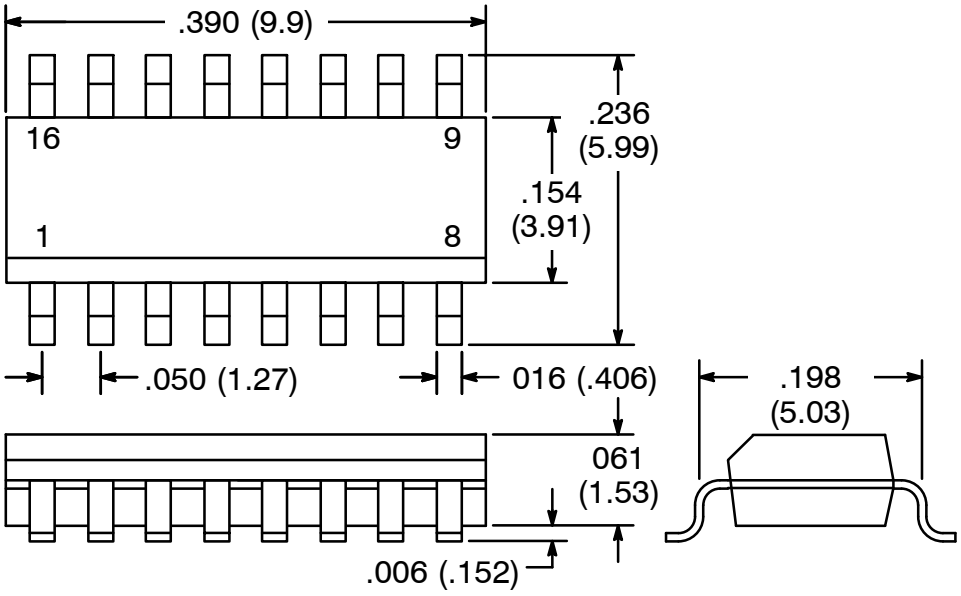


NTE4044BT



NOTE: Pin1 on Beveled Edge