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## NTE4043B & NTE4043BT Integrated Circuit CMOS, Quad NOR R/S Latch

**Description:**

The NTE4043B (16-Lead DIP) and NTE4043BT (SOIC-16) are R-S latch devices constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three-state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

**Features:**

- Double Diode Input Protection
- Three-State Outputs with Common Enable
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range: 3Vdc to 18Vdc

**Absolute Maximum Ratings:** (Voltages referenced to  $V_{SS}$ , Note 1)

DC Supply Voltage, $V_{DD}$ .....	-0.5 to +18.0V
Input Voltage (DC or Transient), $V_{in}$ .....	-0.5 to $V_{DD}$ to +0.5V
Output Voltage (DC or Transient), $V_{out}$ .....	-0.5 to $V_{DD}$ to +0.5V
Input Current (DC or Transient, Per Pin), $I_{in}$ .....	$\pm 10$ mA
Output Current (DC or Transient, Per Pin), $I_{out}$ .....	$\pm 10$ mA
Power Dissipation (Per Package), $P_D$ .....	500mW
Temperature Derating (from +65° to +125°C) .....	-7.0mW/°C
Ambient Temperature Range, $T_A$ .....	-55° to +125°C
Storage Temperature Range, $T_{stg}$ .....	-65° to +150°C
Lead Temperature (During Soldering, 8sec max), $T_L$ .....	+260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

**Electrical Characteristics:** (Voltages referenced to  $V_{SS}$ , Note 2)

Parameter	Symbol	$V_{DD}$ Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0  "1" Level $V_{in} = 0$ or $V_{DD}$	$V_{OL}$	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	Vdc
		15	-	0.05	-	0	0.05	-	0.05	Vdc
	$V_{OH}$	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	Vdc
		15	14.95	-	14.95	15	-	14.95	-	Vdc
Input Voltage "0" Level ( $V_O = 4.5$ or $0.5$ Vdc) ( $V_O = 9.0$ or $1.0$ Vdc) ( $V_O = 13.5$ or $1.5$ Vdc)  "1" Level ( $V_O = 0.5$ or $4.5$ Vdc) ( $V_O = 1.0$ or $9.0$ Vdc) ( $V_O = 1.5$ or $13.5$ Vdc)	$V_{IL}$	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	Vdc
		15	-	4.0	-	6.75	4.0	-	4.0	Vdc
	$V_{IH}$	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	Vdc
		15	11.0	-	11.0	8.25	-	11.0	-	Vdc
Output Drive Current Source ( $V_{OH} = 2.5$ Vdc) ( $V_{OH} = 4.6$ Vdc) ( $V_{OH} = 9.5$ Vdc) ( $V_{OH} = 13.5$ Vdc)  Sink ( $V_{OL} = 0.4$ Vdc) ( $V_{OL} = 0.5$ Vdc) ( $V_{OL} = 1.5$ Vdc)	$I_{OH}$	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	mAdc
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	mAdc
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	mAdc
	$I_{OL}$	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	mAdc
		15	4.2	-	3.4	8.8	-	2.4	-	mAdc
Input Current	$I_{in}$	15	-	±0.1	-	±0.00001	±0.1	-	±0.1	μAdc
Input Capacitance ( $V_{IN} = 0$ )	$C_{in}$	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	$I_{DD}$	5.0	-	1.0	-	0.002	1.0	-	30	μAdc
		10	-	2.0	-	0.004	2.0	-	60	μAdc
		15	-	4.0	-	0.006	4.0	-	120	μAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L = 50$ pF on all outputs all buffers switching, Note 3, Note 4)	$I_T$	5.0	$I_T = (0.58\mu A/kHz) f + I_{DD}$							μAdc
		10	$I_T = (1.15\mu A/kHz) f + I_{DD}$							μAdc
		15	$I_T = (1.73\mu A/kHz) f + I_{DD}$							μAdc
Three-State Output Leakage Current	$I_{TL}$	15	-	±0.1	-	±0.0001	±0.1	-	±0.1	μAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

where:  $I_T$  is in μA (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.004$ .

**Switching Characteristics:** ( $C_L = 50\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , Note 2, Note 3)

Parameter	Symbol	V <sub>DD</sub> Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{PHL} = (1.35\text{ns/pf}) C_L + 32.5\text{ns}$ $t_{TLH}, t_{PHL} = (0.60\text{ns/pf}) C_L + 20\text{ns}$ $t_{TLH}, t_{PHL} = (0.40\text{ns/pf}) C_L + 20\text{ns}$	$t_{TLH},$ $t_{PHL}$	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (0.90\text{ns/pf}) C_L + 130\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pf}) C_L + 57\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pf}) C_L + 47\text{ns}$	$t_{PLH},$ $t_{PHL}$	5.0	–	175	350	ns
		10	–	75	175	ns
		15	–	60	120	ns
Set, $\overline{\text{Set}}$ Pulse Width	$t_W$	5.0	200	80	–	ns
		10	100	40	–	ns
		15	70	30	–	ns
Reset, $\overline{\text{Reset}}$ Pulse Width	$t_W$	5.0	200	80	–	ns
		10	100	40	–	ns
		15	70	30	–	ns
Three-State Enable/Disable Delay	$t_{PLZ},$ $t_{PHZ},$ $t_{PZL},$ $t_{PZH}$	5.0	–	150	300	ns
		10	–	80	160	ns
		15	–	55	110	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

**Truth Table:**

Q	S	R	E
High Impedance	X	X	0
No Change	0	0	1
0	0	1	1
1	1	0	1
1	1	1	1

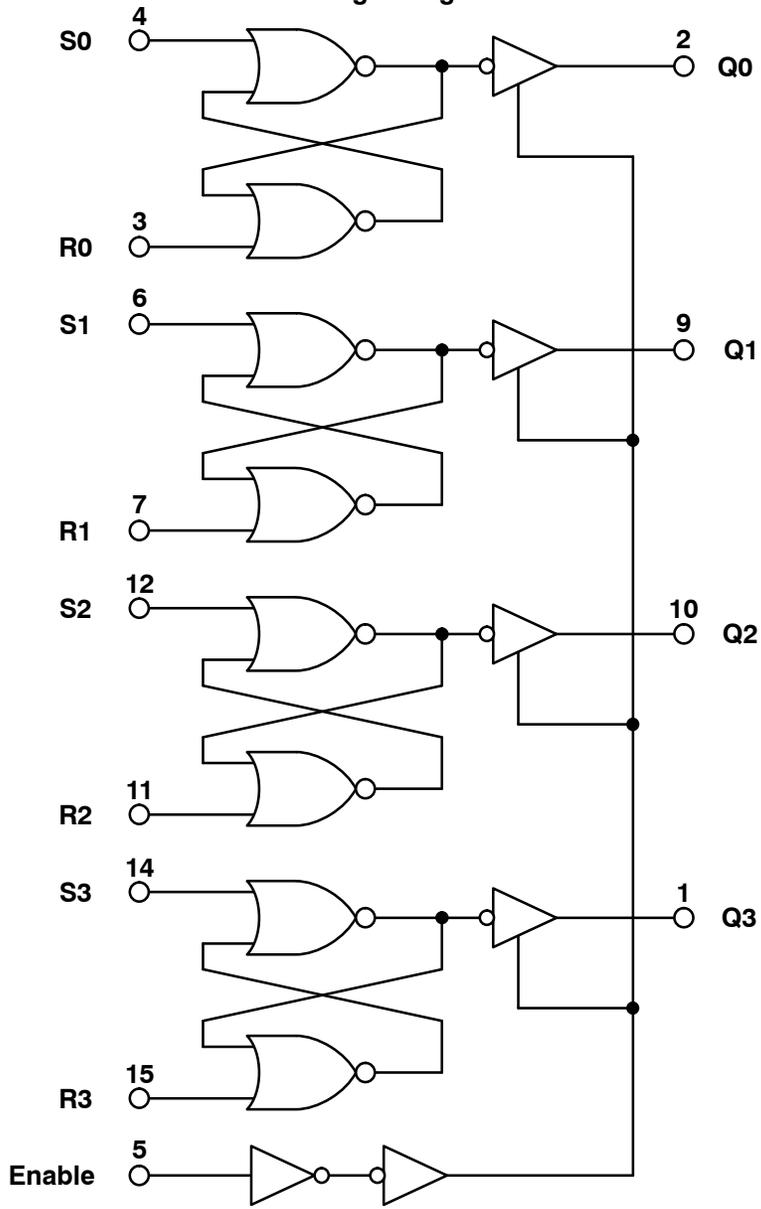
X = Don’t Care

**Three-State Enable/Disable Delays:**

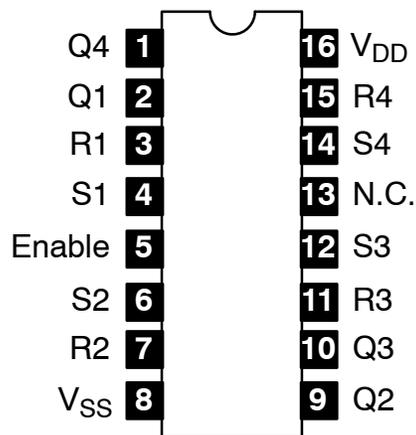
**Set, Reset, Enable, and Switch Conditions for 3-State Tests**

Test	Enable	S1	S2	Q	S	R
$t_{PZH}$		Open	Closed	A	V <sub>DD</sub>	V <sub>SS</sub>
$t_{PZL}$		Closed	Open	B	V <sub>SS</sub>	V <sub>DD</sub>
$t_{PHZ}$		Open	Closed	A	V <sub>DD</sub>	V <sub>SS</sub>
$t_{PLZ}$		Closed	Open	B	V <sub>SS</sub>	V <sub>DD</sub>

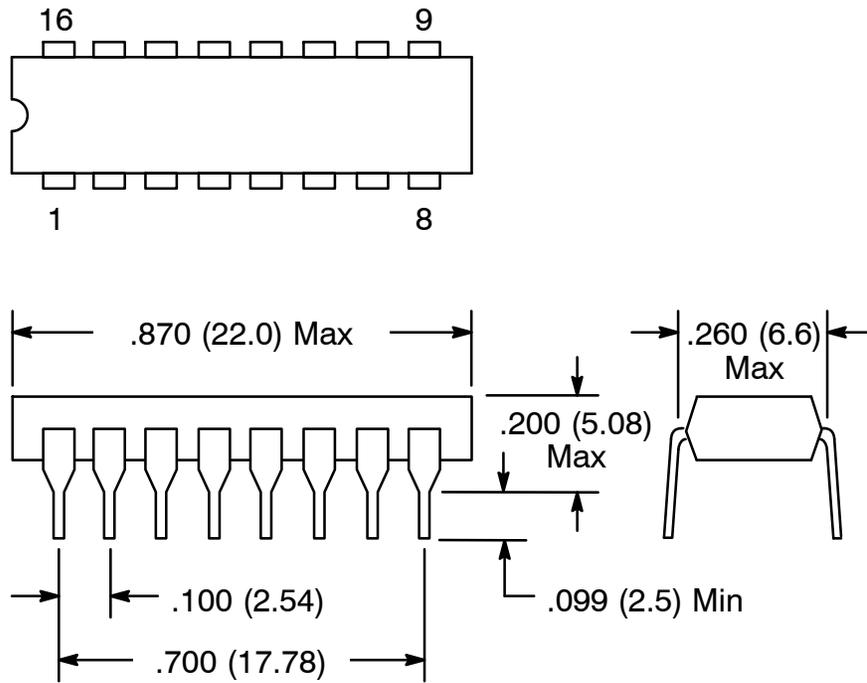
### Logic Diagram



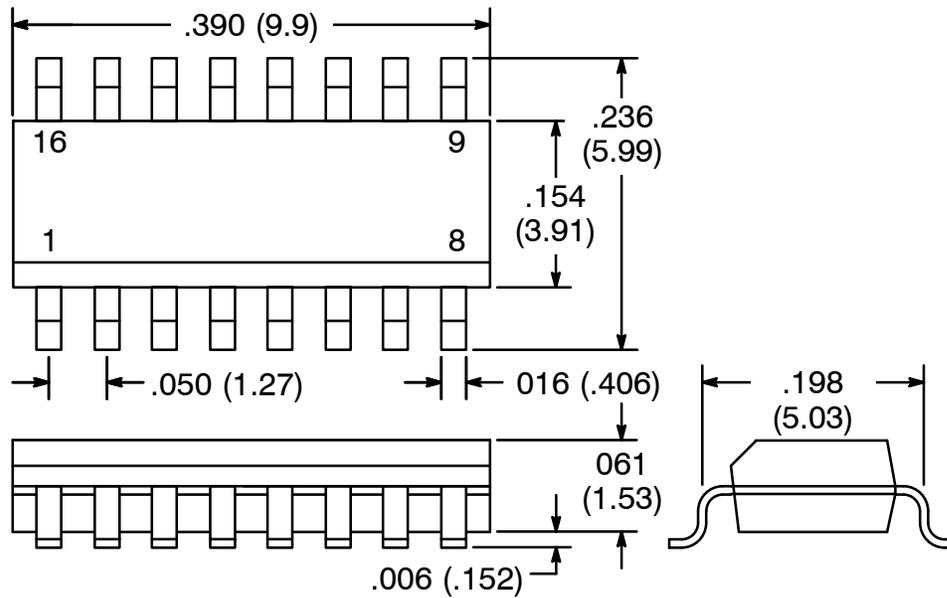
### Pin Connection Diagram



NTE4043B



NTE4043BT



NOTE: Pin1 on Beveled Edge