ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4040B and NTE4040BT
Integrated Circuit
CMOS, 12–Stage Ripple–Carry Binary Counter/Divider

Description:

The NTE4040B (16–Lead DIP) and NTE4040BT (SOIC–16) are 12–stage binary counter constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic package. These device are designed with an input wave shaping circuit and 12 stages of ripple–carry binary counter. The device advances the count on the negative–going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency–driving circuits.

Features:

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range: 3V to 18V
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Common Reset Line

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V

Input or Output Voltage (DC or Transient), V_{in}, V_{out} . . . . . –0.5 to V_{DD}+0.5V

Input or Output Current, per Pin (DC or Transient), I_{in}, I_{out} . . . . . ±10mA

Power Dissipation (per Package), P_D 500mW

Derate Above +65°C . . . . . –7mW/°C

Operating Temperature Range, T_{opr} . . . . . –55° to +125°C

Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Lead Temperature (During Soldering, 8sec), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Note 2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

Electrical Characteristics: (Voltages Referenced to V_{SS}, Note 3)

Parameter	Symbol	V_{DD}	−40°C		+25°C			+85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output "0" Level Voltage V_{in} = V_{DD} or 0	V_{OL}	5	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	V
		15	–	0.05	–	0	0.05	–	0.05	V
Output "1" Level Voltage V_{in} = 0 or V_{DD}	V_{OH}	5	4.95	–	4.95	5	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	V
		15	14.95	–	14.95	15	–	14.95	–	V
Input "0" Level Voltage V_O = 4.5V or 0.5V	V_{IL}	5	–	1.5	–	2.25	1.5	–	1.5	V
V_O = 9.0V or 1.0V		10	–	3.0	–	4.50	3.0	–	3.0	V
V_O = 13.5V or 1.5V		15	–	4.0	–	6.75	4.0	–	4.0	V
Input "1" Level Voltage V_O = 0.5V or 4.5V	V_{IH}	5	3.5	–	3.5	2.75	–	3.5	–	V
V_O = 1.0V or 9.0V		10	7.0	–	7.0	5.50	–	7.0	–	V
V_O = 1.5V or 13.5V		15	11.0	–	11.0	8.25	–	11.0	–	V
Output Drive Source Current V_{OH} = 2.5V	I_{OH}	5	–2.5	–	–2.1	–4.2	–	–1.7	–	mA
V_{OH} = 4.6V		5	–0.52	–	–0.44	–0.88	–	–0.36	–	mA
V_{OH} = 9.5V		10	–1.3	–	–1.1	–2.25	–	–0.9	–	mA
V_{OH} = 13.5V		15	–3.6	–	–3.0	–8.8	–	–2.4	–	mA
Output Drive Sink Current V_{OL} = 0.4V	I_{OL}	5	0.52	–	0.44	0.88	–	0.36	–	mA
V_{OL} = 0.5V		10	1.3	–	1.1	2.25	–	0.9	–	mA
V_{OL} = 1.5V		15	3.6	–	3.0	8.8	–	2.4	–	mA
Input Current	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µA
Input Capacitance, V_{in} = 0	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, Per Package	I_{DD}	5	–	20	–	0.005	20	–	150	µA
		10	–	40	–	0.010	40	–	300	µA
		15	–	80	–	0.015	80	–	600	µA
Total Supply Current Dynamic plus Quiescent, Per Package C_L = 50pF on all outputs, all buffers switching (Note 4)	I_T	5	I_T = (0.42µA/kHz) f + I_{DD}							µA
		10	I_T = (0.85µA/kHz) f + I_{DD}							µA
		15	I_T = (1.43µA/kHz) f + I_{DD}							µA

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA, C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 3, Note 5)

Parameter	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (1.5ns/pF) C_L + 25ns	t_{TLH}	5	–	100	200	ns
t_{TLH} = (0.75ns/pF) C_L +12.5ns		10	–	50	100	ns
t_{TLH} = (0.55ns/pF) C_L + 9.5ns		15	–	40	80	ns
Output Fall Time t_{THL} = (1.5ns/pF) C_L + 25ns	t_{THL}	5	–	100	200	ns
t_{THL} = (0.75ns/Pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pF) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, Clock to Q1 t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 315ns	t_{PLH}, t_{PHL}	5	–	260	520	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 137ns		10	–	115	230	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 95ns		15	–	80	160	ns
Propagation Delay Time, Clock to Q12 t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 2415ns	t_{PLH}, t_{PHL}	5	–	1625	3250	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 867ns		10	–	720	1440	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 475ns		15	–	500	1000	ns
Propagation Delay Time, A_{in}, Reset to Q_n t_{PHL} = (1.7ns/pF) C_L + 485ns	t_{PHL}	5	–	370	740	ns
t_{PHL} = (0.66ns/pF) C_L + 182ns		10	–	155	310	ns
t_{PHL} = (0.5ns/pF) C_L + 145ns		15	–	115	230	ns
Clock Pulse Width	t_{WH}	5	385	140	–	ns
		10	150	55	–	ns
		15	115	38	–	ns
Clock Pulse Frequency	f_{cl}	5	–	2.1	1.5	MHz
		10	–	7.0	3.5	MHz
		15	–	10.0	4.5	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5	No Limit			ns
		10				ns
		15				ns
Reset Pulse Width	t_{WH}	5	960	320	–	ns
		10	360	120	–	ns
		15	270	80	–	ns
Reset Removal Time	t_{rem}	5	130	65	–	ns
		10	50	25	–	ns
		15	30	15	–	ns

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

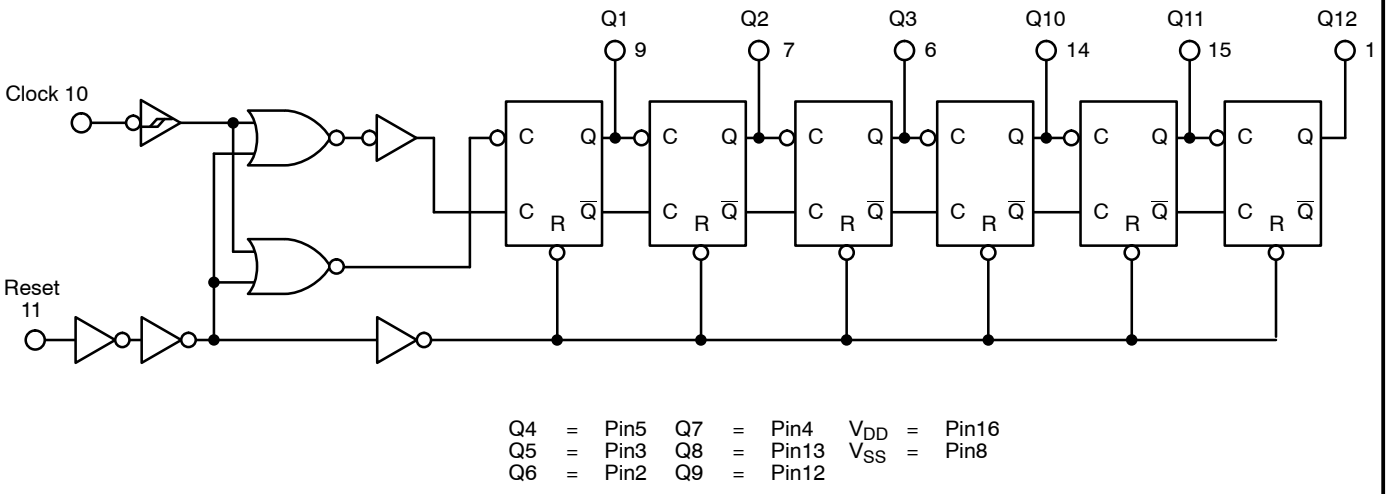
Note 5. The formulas given are for the typical characteristics only at +25°C.

Truth Table

CLOCK	RESET	OUTPUT STATE
⟋	0	No Change
⟍	0	Advance to Next State
X	1	All Outputs are Low

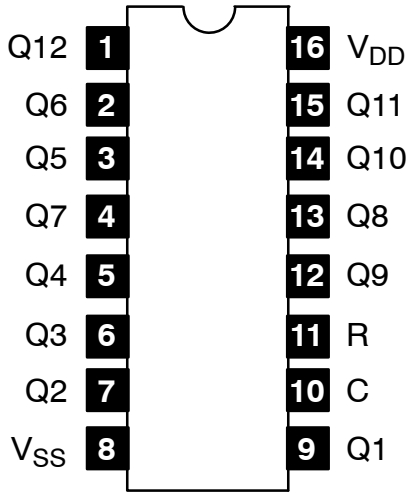
X = Don't Care

Logic Diagram

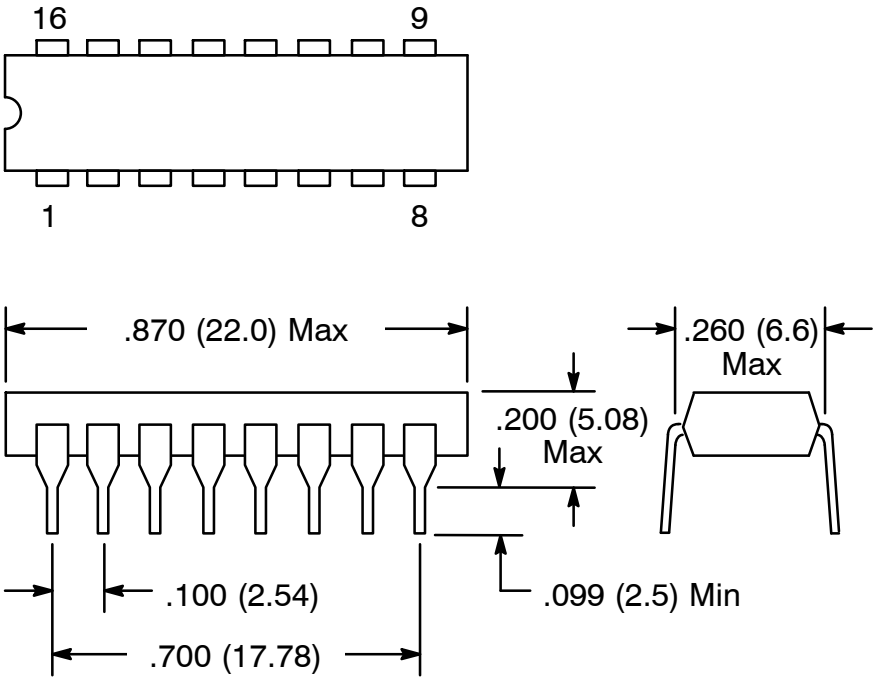


Q4 = Pin5 Q7 = Pin4 V_{DD} = Pin16
Q5 = Pin3 Q8 = Pin13 V_{SS} = Pin8
Q6 = Pin2 Q9 = Pin12

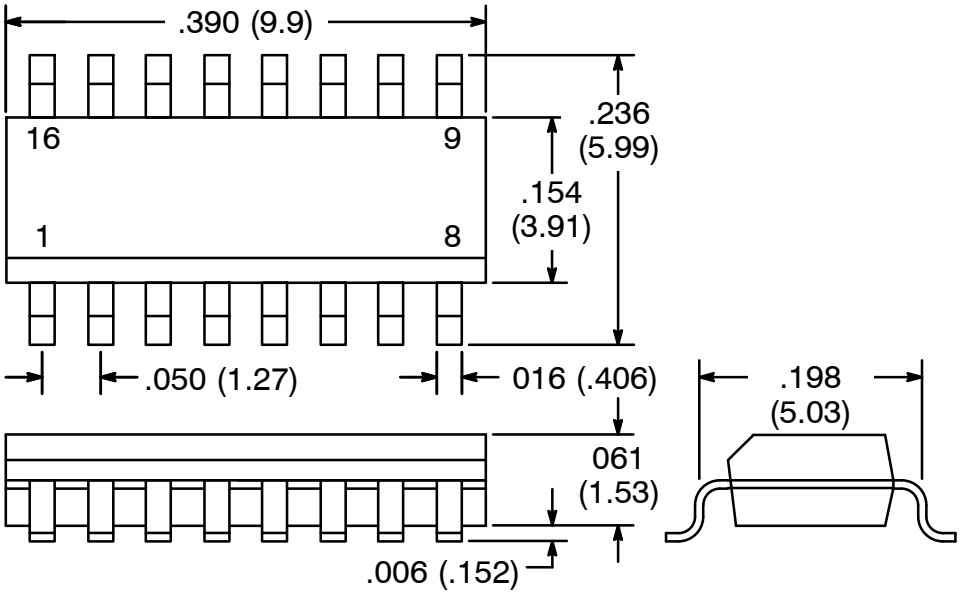
Pin Connection Diagram



NTE4040B



NTE4040BT



NOTE: Pin1 on Beveled Edge