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NTE4029B & NTE4029BT
Integrated Circuit
CMOS, Binary/Decade Up/Down Counter

Description:

The NTE4029B (16–Lead DIP) and NTE4029BT (SOIC–16) Binary/Decade up/down counters are constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip–flop stages with a gating structure to provide toggle flip–flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Internally Synchronous for High Speed
- Logic Edge–Clocked Design — Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Storage Temperature, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	50	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current	I_T	5.0	I_T = (0.58µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 4)		10	I_T = (1.20µA/kHz) f + I_{DD}							µAdc
		15	I_T = (1.70µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					
t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
Clock to Q						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 230ns		5.0	–	200	400	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 97ns		10	–	100	200	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 75ns		15	–	90	180	ns
Clock to $\overline{C_{out}}$						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 230ns		5.0	–	250	500	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 97ns		10	–	130	260	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 75ns		15	–	85	190	ns
$\overline{C_{in}}$ to $\overline{C_{out}}$						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 95ns		5.0	–	175	360	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 47ns		10	–	50	120	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 35ns		15	–	50	100	ns
PE to Q						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 230ns		5.0	–	235	470	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 97ns		10	–	100	200	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 75ns		15	–	80	160	ns
PE to $\overline{C_{out}}$						
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 465ns		5.0	–	320	640	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 192ns		10	–	145	290	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 125ns		15	–	105	210	ns
Clock Pulse Width	$T_{W(cl)}$	5.0	180	90	–	ns
		10	80	40	–	ns
		15	60	30	–	ns
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	2.0	MHz
		10	–	8.0	4.0	MHz
		15	–	10.0	5.0	MHz
Preset Removal Time	t_{rem}	5.0	160	80	–	ns
The Preset Signal must be low prior to a positive−going transition of the clock.		10	80	40	–	ns
		15	60	30	–	ns
Clock Rise and Fall Time	$t_{r(cl)}$, $t_{f(cl)}$	5.0	–	–	15	μs
		10	–	–	5.0	μs
		15	–	–	4.0	μs

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Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Setup Times	t_{su}					
$\overline{\text{Carry In}}$ Setup Time		5.0	150	75	–	ns
		10	60	30	–	ns
		15	40	20	–	ns
Up/Down Setup Time		5.0	340	170	–	ns
		10	140	70	–	ns
		15	100	50	–	ns
Binary/Decade Setup Time		5.0	320	160	–	ns
		10	140	70	–	ns
		15	100	50	–	ns
Preset Enable Pulse Width	t_W	5.0	130	65	–	ns
		10	70	35	–	ns
		15	50	25	–	ns

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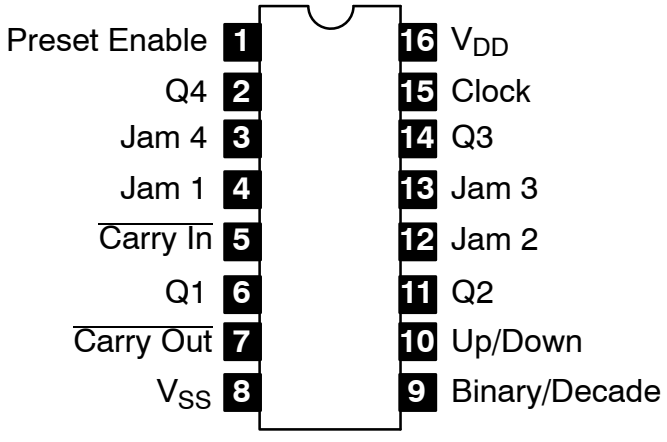
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

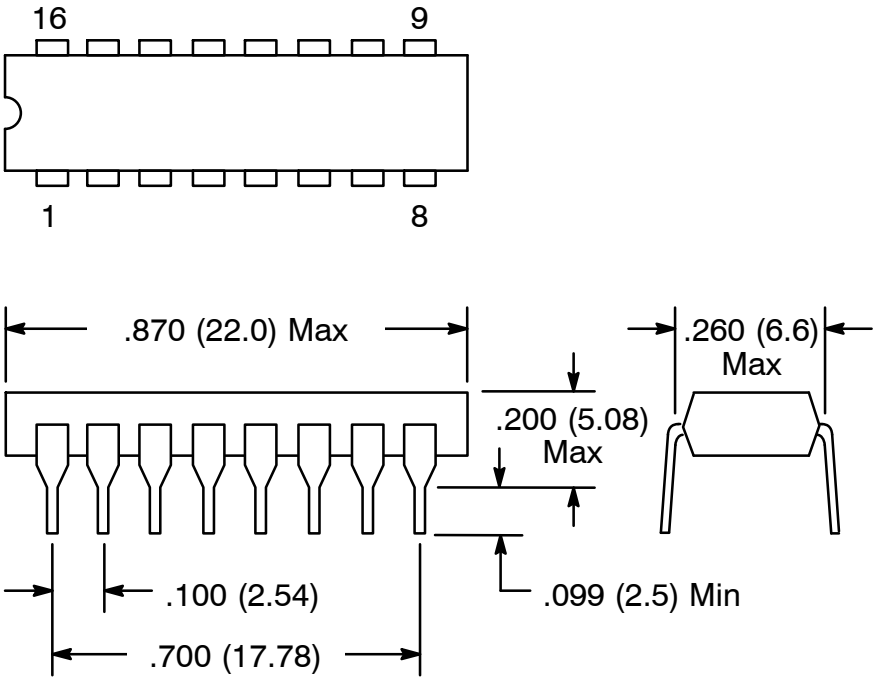
$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don’t Care

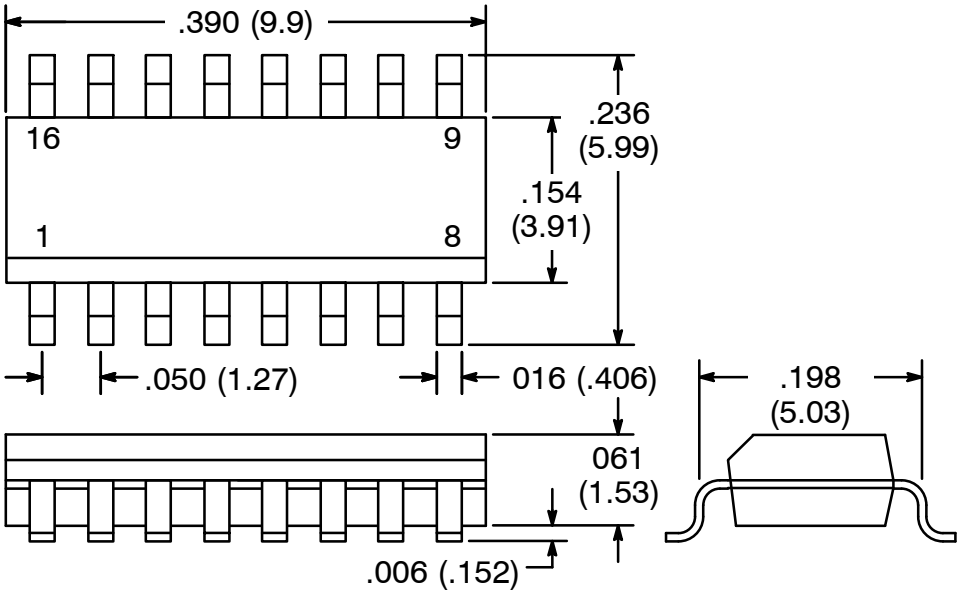
Pin Connection Diagram



NTE4029B



NTE4029BT



NOTE: Pin1 on Beveled Edge