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NTE4020B & NTE4020BT Integrated Circuit CMOS, 14-Bit Binary Counter

Description:

The NTE4020B (16-Lead DIP) and NTE4020BT (SOIC-16) are 14-stage binary counter devices constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These devices are designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

Features:

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 1 and 4 Through 14
- Common Reset Line

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	-0.5 to +18.0V
Input Voltage (DC or Transient), V_{in}	-0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out}	-0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in}	± 10 mA
Output Current (DC or Transient, Per Pin), I_{out}	± 10 mA
Power Dissipation (Per Package), P_D	500mW
Temperature Derating (from +65° to +125°C)	-7.0mW/°C
Storage Temperature, T_{stg}	-65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L	+260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS} , Note 2)

Parameter	Symbol	V_{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0 "1" Level $V_{in} = 0$ or V_{DD}	V_{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		10	-	0.05	-	0	0.05	-	0.05	Vdc
		15	-	0.05	-	0	0.05	-	0.05	Vdc
	V_{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10	-	9.95	-	Vdc
		15	14.95	-	14.95	15	-	14.95	-	Vdc
Input Voltage "0" Level ($V_O = 4.5$ or $0.5V_{dc}$) ($V_O = 9.0$ or $1.0V_{dc}$) ($V_O = 13.5$ or $1.5V_{dc}$) "1" Level ($V_O = 0.5$ or $4.5V_{dc}$) ($V_O = 1.0$ or $9.0V_{dc}$) ($V_O = 1.5$ or $13.5V_{dc}$)	V_{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
		10	-	3.0	-	4.50	3.0	-	3.0	Vdc
		15	-	4.0	-	6.75	4.0	-	4.0	Vdc
	V_{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
		10	7.0	-	7.0	5.50	-	7.0	-	Vdc
		15	11.0	-	11.0	8.25	-	11.0	-	Vdc
Output Drive Current Source ($V_{OH} = 2.5V_{dc}$) ($V_{OH} = 4.6V_{dc}$) ($V_{OH} = 9.5V_{dc}$) ($V_{OH} = 13.5V_{dc}$) Sink ($V_{OL} = 0.4V_{dc}$) ($V_{OL} = 0.5V_{dc}$) ($V_{OL} = 1.5V_{dc}$)	I_{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	mAdc
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	mAdc
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	mAdc
	I_{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	mAdc
15		4.2	-	3.4	8.8	-	2.4	-	mAdc	
Input Current	I_{in}	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 0.1	μ Adc
Input Capacitance ($V_{IN} = 0$)	C_{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)	I_{DD}	5.0	-	5.0	-	0.005	5.0	-	150	μ Adc
		10	-	10	-	0.010	10	-	300	μ Adc
		15	-	20	-	0.015	20	-	600	μ Adc
Total Supply Current (Dynamic plus Quiescent, Per Package, $C_L = 50pF$ on all outputs, all buffers switching, Note 3, Note 4)	I_T	5.0	$I_T = (0.42\mu A/kHz) f + I_{DD}$							μ Adc
		10	$I_T = (0.85\mu A/kHz) f + I_{DD}$							μ Adc
		15	$I_T = (1.43\mu A/kHz) f + I_{DD}$							μ Adc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001$.



Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5\text{ns/pf}) C_L + 25\text{ns}$ $t_{TLH}, t_{THL} = (0.75\text{ns/pf}) C_L + 12.5\text{ns}$ $t_{TLH}, t_{THL} = (0.55\text{ns/pf}) C_L + 9.5\text{ns}$	$t_{TLH},$ t_{THL}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Propagation Delay Time Clock to Q1 $t_{PLH}, t_{PHL} = (0.90\text{ns/pf}) C_L + 115\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pf}) C_L + 47\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pf}) C_L + 37\text{ns}$ Clock to Q14 $t_{PLH}, t_{PHL} = (0.90\text{ns/pf}) C_L + 115\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pf}) C_L + 47\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pf}) C_L + 37\text{ns}$	$t_{PLH},$ t_{PHL}	5.0	–	260	520	ns
		10	–	115	230	ns
		15	–	80	160	ns
		5.0	–	1820	3900	ns
		10	–	805	1725	ns
		15	–	560	1200	ns
Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7\text{ns/pf}) C_L + 285\text{ns}$ $t_{PHL} = (0.66\text{ns/pf}) C_L + 122\text{ns}$ $t_{PHL} = (0.5\text{ns/pf}) C_L + 90\text{ns}$	t_{PHL}	5.0	–	370	740	ns
		10	–	155	310	ns
		15	–	115	230	ns
Clock Pulse Width	t_{WH}	5.0	500	140	–	ns
		10	165	55	–	ns
		15	125	38	–	ns
Clock Pulse Frequency	f_{CL}	5.0	–	2.0	1.0	MHz
		10	–	6.0	3.0	MHz
		15	–	8.0	4.0	MHz
Clock Rise and Fall Time	$t_{TLH},$ t_{THL}	5.0	No Limit			–
		10				–
		15				–
Reset Pulse Width	t_{WL}	5.0	3000	320	–	ns
		10	550	120	–	ns
		15	420	80	–	ns
Reset Removal Time	t_{rem}	5.0	130	65	–	ns
		10	50	25	–	ns
		15	30	15	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

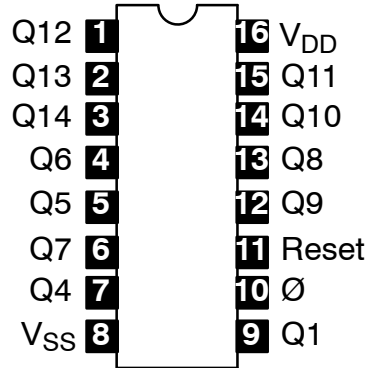
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

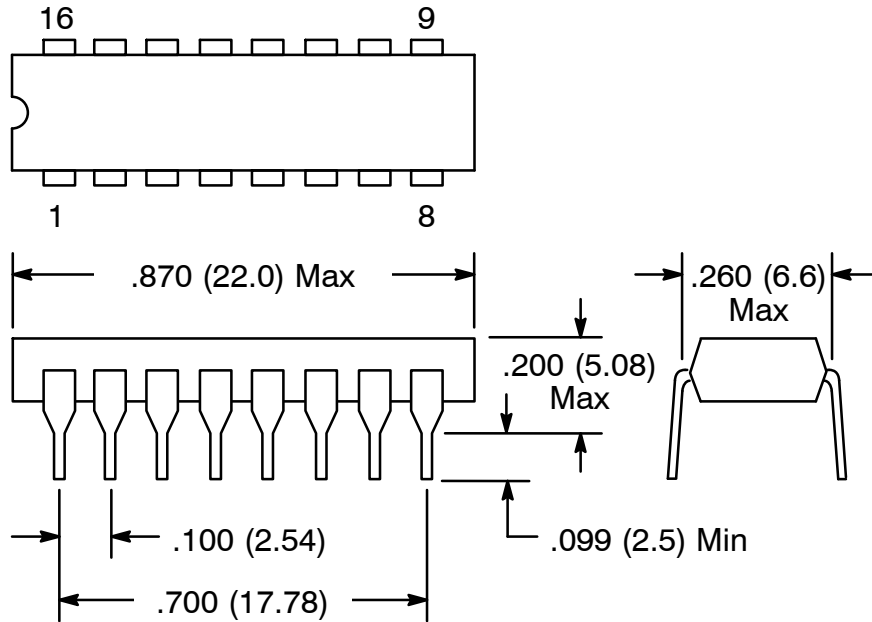
CLOCK	Reset	Output State
	0	No Change
	0	Advance to Next State
X	1	All Outputs are Low

X = Don't care

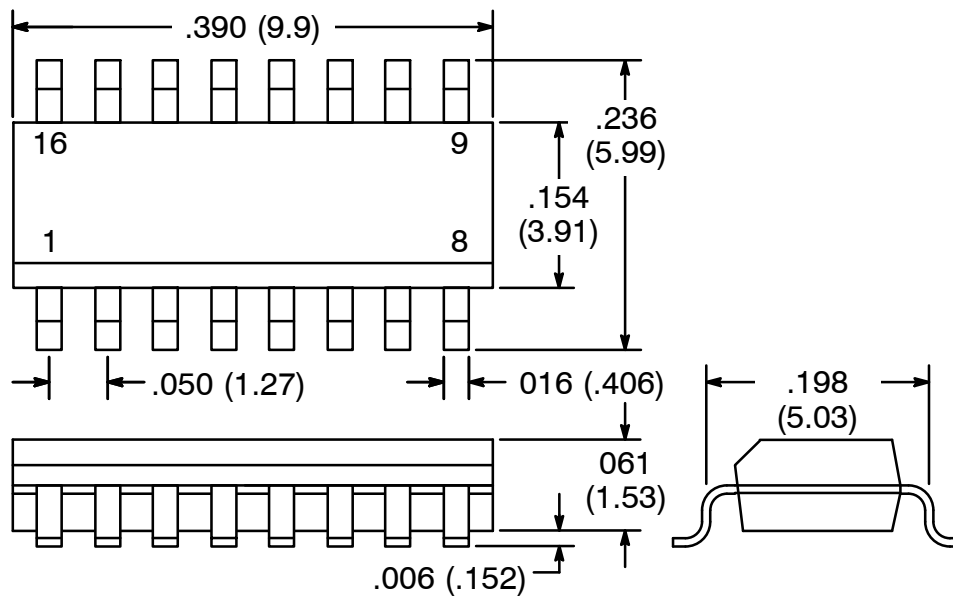
Pin Connection Diagram



NTE4020B



NTE4020BT



NOTE: Pin1 on Beveled Edge