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NTE40192B & NTE40193B
Integrated Circuit
CMOS, Presettable Up/Down Counters
(Dual Clock with Reset)

Description:

The NTE40192B (BCD Type), and NTE40193B (Binary Type) are presettable up/down counters in a 16–Lead DIP type package consisting of 4 synchronously clocked, gated “D” type flip–flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ an $\overline{\text{BORROW}}$ outputs for multiple–stage counting schemes a provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one–half clock cycle after the counter reaches its maximum count in the count–up mode. The $\overline{\text{BORROW}}$ signal goes low one–half clock cycle after the counter reaches its minimum count in the count–down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

Features:

- Individual Clock Lines for Counting Up or Counting Down
- Synchronous High–Speed Carry and Borrow Propagation Delays for Cascading
- Asynchronous Reset and Preset Capability
- Medium–Speed Operation: f_{CL} = 8Mhz (TYP0 at 10V
- 5V, 10V, and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (over Full Package Temperature Range): 1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V

Applications:

- Up/Down Difference Counting
- Multistage Ripple Counting
- Synchronous Frequency Dividers
- A/D and D/A Conversion
- Programmable Binary or BCD Counting

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages Referenced to V_{SS}), V_{DD} . . . . . −0.5 to +20V
Input Voltage Range (All Inputs) . . . . . −0.5 to V_{DD}+0.5V
DC Input Current (Any One Input) . . . . . ±10mA
Power Dissipation (Per Package), P_D
For T_A = −55° to +100°C 500mW
For T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +265°C

Recommended Operating Conditions: (T_A = +25°C, Note 1 unless otherwise specified)

Parameter	V_{DD} (V)	Limits		Unit
		Min	Max	
Supply Voltage Range (Full T_A = Full Package Temperature Range)	–	3	18	V
Removal Time:				
RESET or $\overline{PE}$	5	80	–	ns
	10	40	–	ns
	15	30	–	ns
Pulse Width:				
RESET	5	480	–	ns
	10	300	–	ns
	15	260	–	ns
$\overline{PE}$	5	240	–	ns
	10	170	–	ns
	15	140	–	ns
CLOCK	5	180	–	ns
	10	90	–	ns
	15	60	–	ns
Clock Input Frequency	5		2.0	Mhz
	10	DC	4.0	Mhz
	15		5.5	MHz
Clock Rise or Fall Time	5	–	15	µs
	10	–	15	µs
	15	–	5	µs

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55°C	−40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	µA
	–	0,15	15	20	20	600	600	–	0.04	20	µA
	–	0,20	20	100	100	3000	3000	–	0.08	1000	µA

Static Electrical Characteristics (Cont'd):

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Voltage Low–Level V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input Voltage High–Level V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	V
	1.9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm 10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Operation						
Propagation Delay Time CLOCK UP or CLOCK DOWN to Q, RESET to Q	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	250	500	ns
		V_{DD} = 10V	–	120	240	ns
		V_{DD} = 15V	–	90	180	ns
$\overline{PE}$ to Q		V_{DD} = 5V	–	200	400	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	70	140	ns
CLOCK UP to $\overline{CARRY}$, CLOCK DOWN to $\overline{BORROW}$		V_{DD} = 5V	–	160	320	ns
		V_{DD} = 10V	–	80	160	ns
		V_{DD} = 15V	–	60	120	ns
$\overline{RESET}$ or $\overline{PE}$ to $\overline{BORROW}$ or CARRY		V_{DD} = 5V	–	300	600	ns
		V_{DD} = 10V	–	150	300	ns
		V_{DD} = 15V	–	110	220	ns

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transition Time	t_{THL}, t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Minimum Removal Time (Note 2) RESET or $\overline{PE}$	t_{rem}	V_{DD} = 5V	–	40	80	ns
		V_{DD} = 10V	–	20	40	ns
		V_{DD} = 15V	–	15	30	ns
Minimum Pulse Width RESET	t_W	V_{DD} = 5V	–	240	480	ns
		V_{DD} = 10V	–	150	300	ns
		V_{DD} = 15V	–	130	260	ns
$\overline{PE}$		V_{DD} = 5V	–	120	240	ns
		V_{DD} = 10V	–	85	170	ns
		V_{DD} = 15V	–	70	140	ns
CLOCK		V_{DD} = 5V	–	90	180	ns
		V_{DD} = 10V	–	45	90	ns
		V_{DD} = 15V	–	30	60	ns
Maximum Clock Input Frequency	f_{CL}	V_{DD} = 5V	2.0	4.0	–	MHz
		V_{DD} = 10V	4.0	8.0	–	MHz
		V_{DD} = 15V	5.5	11.0	–	MHz
Clock Rise & Fall Time	t_r, t_f	V_{DD} = 5V	–	–	15	µs
		V_{DD} = 10V	–	–	15	µs
		V_{DD} = 15V	–	–	5	µs
Input Capacitance RESET	C_{IN}	–	–	10	15	pF
All Other Inputs		–	–	5.0	7.5	pF

Note 2. The time required for RESET or $\overline{\text{PRESET ENABLE}}$ control to be removed before clocking.

Truth Table

CLOCK UP	CLOCK DOWN	$\overline{\text{PRESET ENABLE}}$	RESET	Action
⎍	1	1	0	COUNT UP
⎎	1	1	0	NO COUNT
1	⎍	1	0	COUNT DOWN
1	⎎	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	PRESET

1 = High Level
0 = Low Level
X = Don't Care

Pin Connection Diagram