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## NTE40174B & NTE40174BT Integrated Circuit CMOS, Hex D Type Flip-Flop

**Description:**

The NTE40174B (16-Lead DIP) and NTE40174BT (SOIC-16) consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0".

All inputs are protected from static discharge by diode clamps to  $V_{DD}$  and  $V_{SS}$ .

**Features:**

- Wide Supply Voltage Range: 3V to 15V
- High Noise Immunity:  $0.45 V_{DD}$  (Typ)
- Low Power TTL Compatibility: Fan Out of 2 Driving 74L or 1 Driving 74LS

**Absolute Maximum Ratings:** ( $V_{SS} = 0V$ , Note 1 unless otherwise specified)

DC Supply Voltage, $V_{DD}$	.....	-0.5 to +18.0V
Input Voltage, $V_{IN}$	.....	-0.5 to $V_{DD}$ to +0.5V
Power Dissipation, $P_D$	.....	700mW
Storage Temperature Range, $T_{stg}$	.....	-65° to +150°C
Lead Temperature (During Soldering, 10sec max), $T_L$	.....	+260°C

Note 1. "Absolute Maximum Ratings" are those values beyond which the safety of the devices cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Absolute Maximum Ratings:** ( $V_{SS} = 0V$  unless otherwise specified)

DC Supply Voltage, $V_{DD}$	.....	3 to +15.0V <sub>DC</sub>
Input Voltage, $V_{IN}$	.....	0 to $V_{DD}$ V <sub>DC</sub>
Operating Temperature Range, $T_A$	.....	-55° to +125°C

**DC Electrical Characteristics:** ( $V_{SS} = 0V$  unless otherwise specified)

Parameter	Symbol	$V_{DD}$ Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Quiescent Device Current $V_{in} = V_{DD}$ or $V_{SS}$	$I_{DD}$	5.0	-	1.0	-	-	1.0	-	30	$\mu$ Adc
		10	-	2.0	-	-	2.0	-	60	$\mu$ Adc
		15	-	4.0	-	-	4.0	-	120	$\mu$ Adc
Low Level Output Voltage ( $ I_O  < 1\mu A$ )	$V_{OL}$	5.0	-	0.05	-	-	0.05	-	0.05	Vdc
		10	-	0.05	-	-	0.05	-	0.05	Vdc
		15	-	0.05	-	-	0.05	-	0.05	Vdc
High Level Output Voltage ( $ I_O  < 1\mu A$ )	$V_{OH}$	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		10	9.95	-	9.95	10.0	-	9.95	-	Vdc
		15	14.95	-	14.95	15.0	-	14.95	-	Vdc
Low Level Input Voltage ( $V_O = 0.5$ or $4.5Vdc$ ) ( $V_O = 1.0$ or $9.0Vdc$ ) ( $V_O = 1.5$ or $13.5Vdc$ )	$V_{IL}$	5.0	-	1.5	-	-	1.5	-	1.5	Vdc
		10	-	3.0	-	-	3.0	-	3.0	Vdc
		15	-	4.0	-	-	4.0	-	4.0	Vdc
High Level Input Voltage ( $V_O = 0.5$ or $4.5Vdc$ ) ( $V_O = 1.0$ or $9.0Vdc$ ) ( $V_O = 1.5$ or $13.5Vdc$ )	$V_{IH}$	5.0	3.5	-	3.5	-	-	3.5	-	Vdc
		10	7.0	-	7.0	-	-	7.0	-	Vdc
		15	11.0	-	11.0	-	-	11.0	-	Vdc
Low Level Output Current (Note 2) ( $V_{OL} = 0.4Vdc$ ) ( $V_{OL} = 0.5Vdc$ ) ( $V_{OL} = 1.5Vdc$ )	$I_{OL}$	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		10	1.6	-	1.3	2.25	-	0.9	-	mAdc
		15	4.2	-	3.4	8.8	-	2.4	-	mAdc
High Level Output Current (Note 2) ( $V_{OH} = 4.6Vdc$ ) ( $V_{OH} = 9.5Vdc$ ) ( $V_{OH} = 13.5Vdc$ )	$I_{OH}$	5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	mAdc
		10	-1.6	-	-1.3	-2.25	-	-0.9	-	mAdc
		15	-4.2	-	-3.4	-8.8	-	-2.4	-	mAdc
Input Current	$I_{IN}$	15	-	$\pm 0.1$	-	$\pm 10^{-5}$	$\pm 0.1$	-	$\pm 1.0$	$\mu$ Adc

Note 2.  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

**AC Electrical Characteristics:** ( $C_L = 50pF$ ,  $R_L = 200k$ ,  $t_r = t_f = 20ns$ ,  $T_A = +25^\circ C$ , Note 3 unless otherwise specified)

Parameter	Symbol	$V_{DD}$ Vdc	Min	Typ	Max	Unit
Propagation Delay Time to a Logical "0" from Clear to Q	$t_{PHL}$	5.0	-	180	300	ns
		10	-	70	110	ns
		15	-	60	90	ns
Time Prior to Clock Pulse that Data must be Present	$t_{SU}$	5.0	-	45	100	ns
		10	-	15	40	ns
		15	-	13	35	ns

Note 3. AC Parameters are guaranteed by DC correlated testing.

**AC Electrical Characteristics (Cont'd):** ( $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}$ ,  $t_r = t_f = 20\text{ns}$ ,  $T_A = +25^\circ\text{C}$ , Note 3 unless otherwise specified)

Parameter	Symbol	$V_{DD}$ Vdc	Min	Typ	Max	Unit
Time After Clock Pulse that Data must be Held	$t_H$	5.0	-	-11	0	ns
		10	-	-4	0	ns
		15	-	-3	0	ns
Transition Time	$t_{THL}$ , $t_{TLH}$	5.0	-	100	200	ns
		10	-	50	100	ns
		15	-	40	80	ns
Minimum Clock Pulse Width	$t_{WH}$ , $t_{WL}$	5.0	-	130	250	ns
		10	-	45	100	ns
		15	-	40	80	ns
Minimum Clear Pulse Width	$t_{WL}$	5.0	-	120	250	ns
		10	-	45	100	ns
		15	-	40	80	ns
Maximum Clock Rise Time	$t_{rCL}$	5.0	15.0	-	-	$\mu\text{s}$
		10	5.0	-	-	$\mu\text{s}$
		15	5.0	-	-	$\mu\text{s}$
Maximum Clock Fall Time	$t_{fCL}$	5.0	15.0	50	-	$\mu\text{s}$
		10	5.0	50	-	$\mu\text{s}$
		15	5.0	50	-	$\mu\text{s}$
Maximum Clock Frequency	$f_{CL}$	5.0	2.0	3.5	-	MHz
		10	5.0	10.0	-	MHz
		15	6.0	12.0	-	MHz
Input Capacitance Clear Input	$C_{IN}$	-	-	10.0	15.0	pF
		-	-	5.0	7.5	pF
Power Dissipation (Per Package, Note 4)	$C_{PD}$	-	-	130	-	pF

Note 3. AC Parameters are guaranteed by DC correlated testing.

Note 4.  $C_{PD}$  determines the no load AC power consumption of any CMOS device.

**Truth Table**

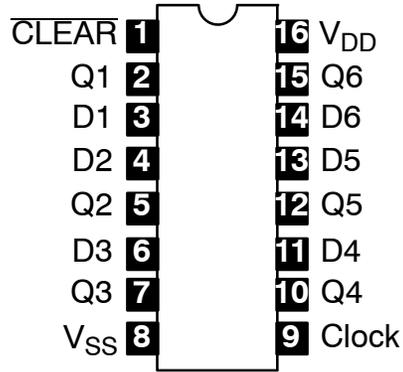
Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H	X	NC
H	L	X	NC

X = Don't Care

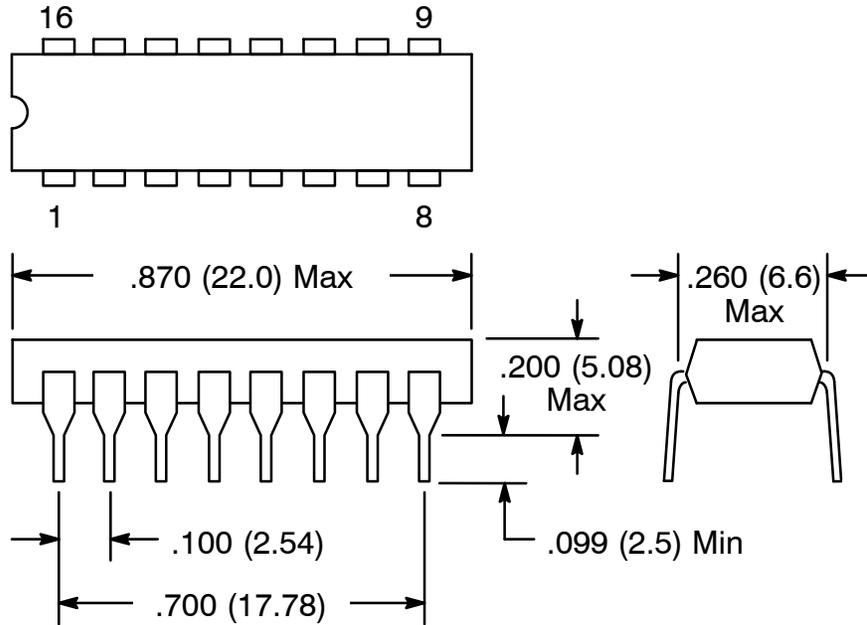
↑ = Transition from Low to High level input

NC = No change

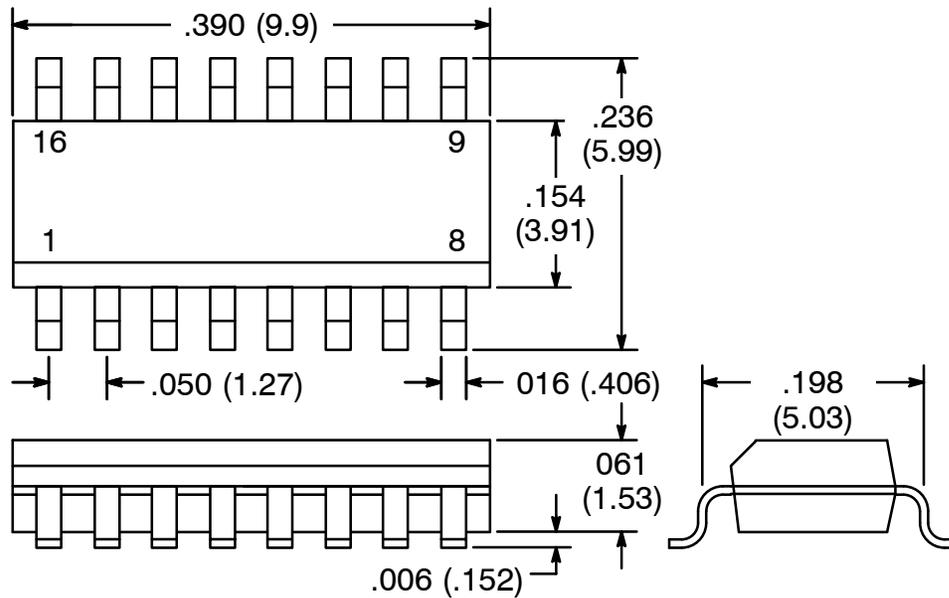
**Pin Connection Diagram**



**NTE40174B**



**NTE40174BT**



NOTE: Pin1 on Beveled Edge