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NTE4015B & NTE4015BT
Integrated Circuit
CMOS, Dual 4–Bit Static Shift Register

Description:

The NTE4015B (16–Lead DIP) and NTE4015BT (SOIC–16) are dual 4–bit static shift registers constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These devices consist of two identical, independent 4–state serial–input/parallel–output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register states are type D master–slave flip–flops. Data is shifted from one stage to the next during the positive–going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial–to–parallel conversion where low power dissipation and/or noise immunity is desired.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Logic Edge–Clocked Flip–Flop Design —
  Logic State is retained Indefinitely with Clock Level either High or Low; Information is Transferred to the Output Only on the Positive Going Edge of the Clock Pulse
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Storage Temperature, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage “0” Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	15	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on All Outputs, All Buffers Switching, Note 3, Note 4)	I_T	5.0	I_T = (1.2µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.4µA/kHz) f + I_{DD}							µAdc
		15	I_T = (3.6µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					
t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
Clock, Data to Q						
t_{PHL}, t_{PLH} = (1.7ns/pf) C_L + 225ns		5.0	–	310	750	ns
t_{PHL}, t_{PLH} = (0.66ns/pf) C_L + 92ns		10	–	125	250	ns
t_{PHL}, t_{PLH} = (0.5ns/pf) C_L + 65ns		15	–	90	170	ns
Reset to Q						
t_{PHL}, t_{PLH} = (1.7ns/pf) C_L + 375ns		5.0	–	460	750	ns
t_{PHL}, t_{PLH} = (0.66ns/pf) C_L + 147ns		10	–	180	250	ns
t_{PHL}, t_{PLH} = (0.5ns/pf) C_L + 95ns		15	–	120	170	ns
Clock Pulse Width	t_{WH}	5.0	400	185	–	ns
		10	175	85	–	ns
		15	135	55	–	ns
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.5	MHz
		10	–	6.0	3.0	MHz
		15	–	7.5	3.75	MHz
Clock Pulse Rise and Fall Times	t_{TLH}, t_{THL}	5.0	–	–	15	µs
		10	–	–	5	µs
		15	–	–	4	µs
Reset Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	160	80	–	ns
		15	120	60	–	ns
Setup Time	t_{su}	5.0	350	100	–	ns
		10	100	50	–	ns
		15	75	40	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

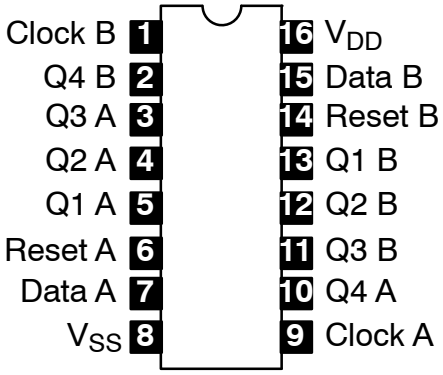
Clock	D	R	Q0	Q_n
⎍	0	0	0	Q_{n-1}
⎍	1	0	1	Q_{n-1}
⎏	X	0	No Change	No Change
X	X	1	0	0

X = Don’t Care

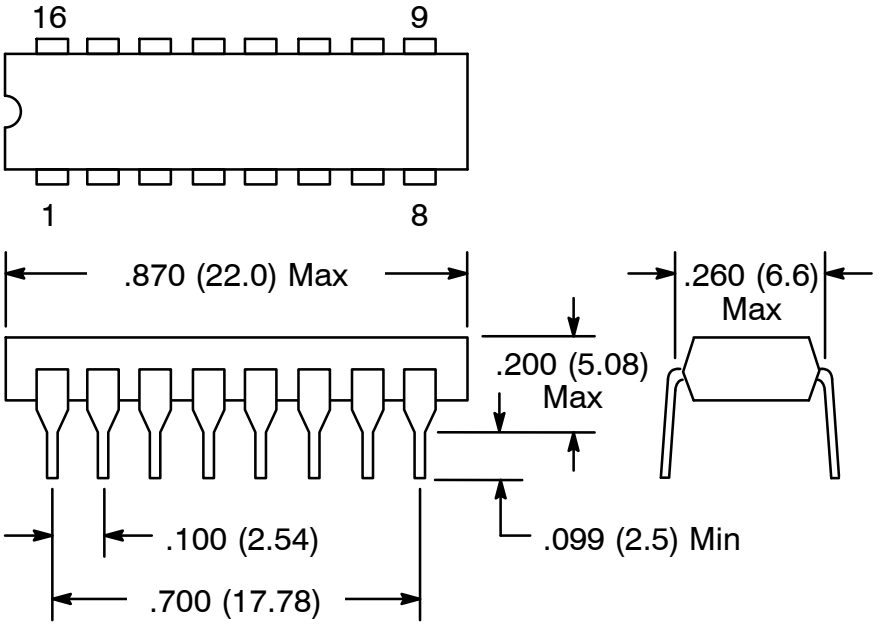
Q_n = Q0, Q1, Q2, or Q3 as applicable

Q_{n-1} = Output of prior stage

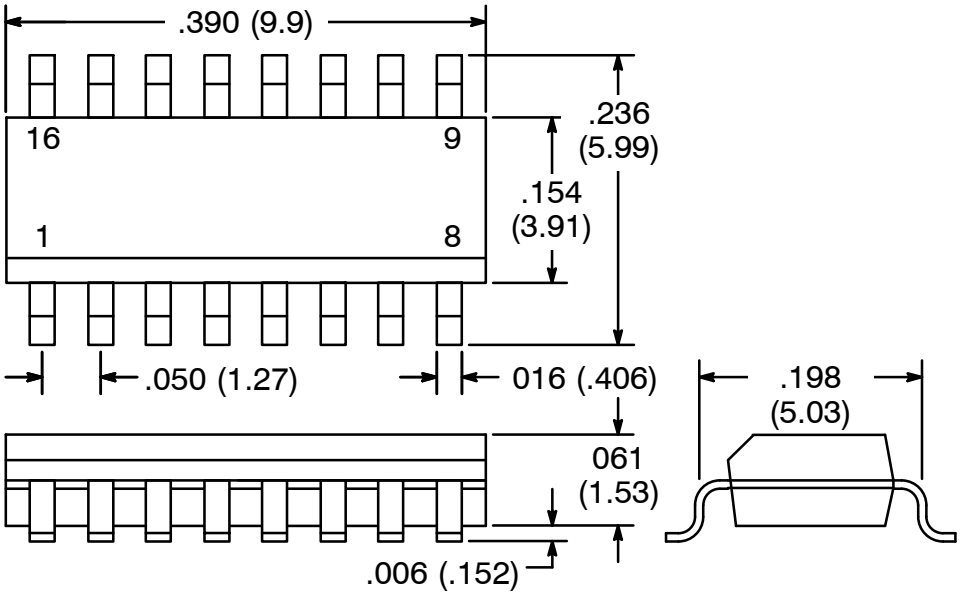
Pin Connection Diagram



NTE4015B



NTE4015BT



NOTE: Pin1 on Beveled Edge