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## NTE27C2001-12D Integrated Circuit 2 Mbit (256Kb x 8) UV EPROM

### **Description:**

The NTE27C2001-12D is an 2 Mbit UV EPROM in a 32-Lead DIP type package ideally suited for applications where fast turn-around and pattern experimentation are important requirements and is organized as 262,144 by 8 bits. This device has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

### **Features:**

- 5V ±10% Supply Voltage in Read Operation
- Access Time: 55ns
- Low Power “CMOS” Consumption:
  - Active Current 35mA at 5MHz
  - Standby Current 100µA
- Programming Voltage: 12.75V ±0.25V
- Programming Time: 100µs/Word

### **Absolute Maximum Ratings:** (Note 1)

Supply Voltage, $V_{CC}$ .....	-2 to +7V
Input or Output Voltage (Except A9, Note 2), $V_{IO}$ .....	-2 to +7V
A9 Voltage (Note 2), $V_{A9}$ .....	-2 to +13.5V
Program Supply Voltage, $V_{PP}$ .....	-2 to +14V
Ambient Operating Temperature Range, $T_A$ .....	-40° to +125°C
Temperature Under Bias Range, $T_{BIAS}$ .....	-50° to +125°C
Storage Temperature Range, $T_{STG}$ .....	-65° to +150°C

Note 1. Except for the rating “Operating Temperature Range”, stresses above those listed in the table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Note 2. Minimum DC voltage on the input or output is -0.5V with possible undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on output is  $V_{CC} + 0.5V$  with possible overshoot to  $V_{CC} + 2V$  for a period less than 20ns.

### **Device Operation:**

The modes of operation of the NTE27C2001 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for  $V_{PP}$  and 12V on A9.

### **Read Mode:**

The NTE27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ( $\bar{E}$ ) is the power control and should be used for device selection. Output Enable ( $\bar{G}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time ( $t_{AVQV}$ ) is equal to the delay from  $\bar{E}$  to output ( $t_{ELQV}$ ). Data is available at the output after a delay of  $t_{GLQV}$  from the falling edge of  $\bar{G}$ , assuming that  $\bar{E}$  has been low and the addresses have been stable for at least  $t_{AVQV} - t_{GLQV}$ .

### **Operating Modes:**

Mode	$\bar{E}$	$\bar{G}$	$\bar{P}$	A9	$V_{PP}$	Q7-Q0
Read	$V_{IL}$	$V_{IL}$	X	X	$V_{CC}$ or $V_{SS}$	Data Out
Output Disable	$V_{IL}$	$V_{IH}$	X	X	$V_{CC}$ or $V_{SS}$	Hi-Z
Program	$V_{IL}$	$V_{IH}$	$V_{IL}$ Pulse	X	$V_{PP}$	Data Input
Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	$V_{PP}$	Data Output
Program Inhibit	$V_{IH}$	X	X	X	$V_{PP}$	Hi-Z
Standby	$V_{IH}$	X	X	X	$V_{CC}$ or $V_{SS}$	Hi-Z

Note: X =  $V_{IH}$  or  $V_{IL}$ ,  $V_{ID} = 12V \pm 0.5V$ .

### **Capacitance:** ( $T_A = +25^\circ C$ , $f = 1MHz$ , Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0V$	-	-	6	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0V$	-	-	12	pF

Note 3. Sampled only, not 100% tested.

### **Standby Mode:**

The NTE27C2001 has a standby mode which reduces the active current from 30mA to 100 $\mu$ A. The NTE27C2001 is placed in the standby mode by applying a CMOS high signal to the  $\bar{E}$  input. When in the standby mode, the outputs are in a high impedance state, independent of the  $\bar{G}$  input.

### **Two Line Output Control:**

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- The lowest possible memory power dissipation,
- Complete assurance that output bus connection will not occur.

For the most efficient use of these two control lines,  $\bar{E}$  should be decoded and used as the primary device selecting function, while  $\bar{G}$  should be made a common connection to all devices in the array and connected to the  $\bar{READ}$  line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

**Read Mode DC Characteristics:** ( $T_A = 0^\circ$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{PP} = V_{CC}$ , Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	$I_{LI}$	$0\text{V} \leq V_{IN} \leq V_{CC}$	–	–	$\pm 10$	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$0\text{V} \leq V_{OUT} \leq V_{CC}$	–	–	$\pm 10$	$\mu\text{A}$
Supply Current	$I_{CC}$	$\bar{E} = V_{IL}$ , $\bar{G} = V_{IL}$ , $I_{OUT} = 0\text{mA}$ , $f = 5\text{MHz}$	–	–	30	$\text{mA}$
Supply Current (Standby) TTL	$I_{CC1}$	$\bar{E} = V_{IH}$	–	–	1	$\text{mA}$
CMOS	$I_{CC2}$	$\bar{E} > V_{CC} - 0.2\text{V}$	–	–	100	$\mu\text{A}$
Program Current	$I_{PP}$	$V_{PP} = V_{CC}$	–	–	10	$\mu\text{A}$
Input Low Voltage	$V_{IL}$		–0.3	–	0.8	$\text{V}$
Input High Voltage	$V_{IH}$	Note 5	2	–	$V_{CC}+1$	$\text{V}$
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	–	–	0.4	$\text{V}$
Output High Voltage TTL	$V_{OH}$	$I_{OH} = -400\mu\text{A}$	2.4	–	–	$\text{V}$
CMOS		$I_{OH} = -100\mu\text{A}$	$V_{CC}-0.7$	–	–	$\text{V}$

Note 4.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

Note 5. Maximum DC voltage on output is  $V_{CC} + 0.5\text{V}$ .

### System Considerations:

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current,  $I_{CC}$ , has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of  $\bar{E}$ . The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a  $0.1\mu\text{F}$  ceramic capacitor be used on every device between  $V_{CC}$  and  $V_{SS}$ . This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a  $4.7\mu\text{F}$  bulk electrolytic capacitor should be used between  $V_{CC}$  and  $V_{SS}$  for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Read Mode AC Characteristics:** ( $T_A = 0^\circ$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ , Note 4 unless otherwise specified)

Parameter	Symbol	Alt.	Test Conditions	Min	Typ	Max	Unit
Address Valid To Output Valid	$t_{AVQV}$	$t_{ACC}$	$\bar{E} = V_{IL}$ , $\bar{G} = V_{IL}$	–	–	120	$\text{ns}$
Chip Enable Low To Output Valid	$t_{ELQV}$	$t_{CE}$	$\bar{G} = V_{IL}$	–	–	120	$\text{ns}$
Output Enable Low To Output Valid	$t_{GLQV}$	$t_{OE}$	$\bar{E} = V_{IL}$	–	–	50	$\text{ns}$
Chip Enable High To Output Hi-Z	$t_{EHQZ}$	$t_{DF}$	$\bar{G} = V_{IL}$ , Note 3	0	–	40	$\text{ns}$
Output Enable High To Output Hi-Z	$t_{GHQZ}$	$t_{DF}$	$\bar{E} = V_{IL}$ , Note 3	0	–	40	$\text{ns}$
Address Transition To Output Transition	$t_{AXQX}$	$t_{OH}$	$\bar{E} = V_{IL}$ , $\bar{G} = V_{IL}$	0	–	–	$\text{ns}$

Note 3. Sampled only, not 100% tested.

Note 4.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

**Programming Mode DC Characteristics:** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$ , Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	$I_{LI}$	$V_{IL} \leq V_{IN} \leq V_{IH}$	-	-	$\pm 10$	$\mu\text{A}$
Supply Current	$I_{CC}$		-	-	50	mA
Program Current	$I_{PP}$	$\bar{E} = V_{IL}$	-	-	50	mA
Input Low Voltage	$V_{IL}$		-0.3	-	0.8	V
Input High Voltage	$V_{IH}$		2	-	$V_{CC} + 0.5$	V
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V
Output High Voltage, TTL	$V_{OH}$	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V
A9 Voltage	$V_{ID}$		11.5	-	12.5	V

Note 4.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

**Programming Mode AC Characteristics:** ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$ , Note 4 unless otherwise specified)

Parameter	Symbol	Alt.	Test Conditions	Min	Typ	Max	Unit
Address Valid To Program Low	$t_{AVPL}$	$t_{AS}$		2	-	-	$\mu\text{s}$
Input Valid To Program Low	$t_{QVPL}$	$t_{DS}$		2	-	-	$\mu\text{s}$
$V_{PP}$ High To Program Low	$t_{VPHPL}$	$t_{OES}$		2	-	-	$\mu\text{s}$
$V_{CC}$ High To Program Low	$t_{VCHPL}$	$t_{VCS}$		2	-	-	$\mu\text{s}$
Chip Enable Low To Program Low	$t_{ELPL}$	$t_{CES}$		2	-	-	$\mu\text{s}$
Program Pulse Width	$t_{PLPH}$	$t_{PW}$		95	-	105	$\mu\text{s}$
Program High To Input Transition	$t_{PHQX}$	$t_{DH}$		2	-	-	$\mu\text{s}$
Input Transition To Output Enable Low	$t_{QXGL}$	$t_{OES}$		2	-	-	$\mu\text{s}$
Output Enable Low To Output Valid	$t_{GLQV}$	$t_{OE}$		-	-	100	ns
Output Enable High To Output Hi-Z	$t_{GHQZ}$	$t_{DFP}$	Note 3	0	-	130	ns
Output Enable High To Address Transition	$t_{GHAX}$	$t_{AH}$		0	-	-	ns

Note 3. Sampled only, not 100% tested.

Note 4.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

### Programming:

When delivered (and after each erasure for UV EPROM), all bits of the NTE27C2001 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The only way to change a "0" to a "1" is by die exposure to ultraviolet light (UV EPROM). The NTE27C2001 is in the programming mode when  $V_{PP}$  input is at 12.75V,  $\bar{E}$  is at  $V_{IL}$  and  $\bar{P}$  is pulsed to  $V_{IL}$ . The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.  $V_{CC}$  is specified to be 6.25V  $\pm$  0.25V.

### Program Inhibit:

Programming of multiple NTE27C2001s in parallel with different data is also easily accomplished. Except for  $\bar{E}$ , all like inputs including  $\bar{G}$  of the parallel NTE27C2001 may be common. A TTL low level pulse applied to an NTE27C2001's  $\bar{P}$  input, with  $\bar{E}$  low and  $V_{PP}$  at 12.75V, will program that NTE27C2001. A high level  $\bar{E}$  input inhibits the other NTE27C2001s from being programmed.

### Program Verify:

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\bar{E}$  and  $\bar{G}$  at  $V_{IL}$ ,  $\bar{P}$  at  $V_{IH}$ ,  $V_{PP}$  at 12.75V and  $V_{CC}$  at 6.25V.

### Erasure Operation:

The erasure characteristics of the NTE27C2001 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately  $4000\text{\AA}$ . It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the  $3000\text{--}4000\text{\AA}$  range. Research shows that constant exposure to room level fluorescent lighting could erase a typical NTE27C2001 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NTE27C2001 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the NTE27C2001 window to prevent unintentional erasure. The recommended erasure procedure for the NTE27C2001 is exposure to short wave ultraviolet light which has a wavelength of  $2537\text{\AA}$ . The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of  $15\text{W}\text{--}\text{sec}/\text{cm}^2$ . The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with  $12000\mu\text{W}/\text{cm}^2$  power rating. The NTE27C2001 should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Pin Connection Diagram



