ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE74HCT74
Integrated Circuit
TTL – High Speed CMOS,
Dual D–Type Flip–Flop with Preset & Clear

Description:

The NTE74HCT74 is an octal D–type flip–flop in a 14–Lead DIP type package that uses advanced silicon–gate CMOS technology to achieve operation speeds similar to the equivalent LS–TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS–TTL loads.

This flip–flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive–going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The NTE74HCT logic family is functionally and pin–out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and GND.

NTE74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These devices are also plug–in replacements to LS–TTL devices and can be used to reduce power consumption in existing designs.

Features:

- Typical Propagation Delay: 20ns
- Low Quiescent Current: 40μA (max)
- Low Input Current: 1μA (max)
- Fanout of 10 LS–TTL Loads

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	5.5	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times	t_r, t_f	–	–	500	ns

DC Electrical Characteristics: (V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions		T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}			–	2.0	2.0	V
Maximum Low Level Input Voltage	V_{IL}			–	0.8	0.8	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\|$ = 20μA	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			$\|I_{OUT}\|$ = 4.0mA, V_{CC} = 4.5V	4.2	3.98	3.84	V
			$\|I_{OUT}\|$ = 4.8mA, V_{CC} = 5.5V	5.2	4.98	4.84	V
Maximum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	$\|I_{OUT}\|$ = 20μA	0	0.1	0.1	V
			$\|I_{OUT}\|$ = 4.0mA, V_{CC} = 4.5V	0.2	0.26	0.33	V
			$\|I_{OUT}\|$ = 4.8mA, V_{CC} = 5.5V	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		–	±0.5	±0.5	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		–	2.0	20	μA
		V_{IN} = 2.4V or 0.5V, Note 4		–	0.3	0.4	mA

Note 4. This is measured per input with all other inputs held at V_{CC} or GND.

AC Electrical Characteristics: (V_{CC} = 5V, C_L = 15pF, t_r = t_f = 6ns, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Operating Frequency from Clock to Q or $\overline{Q}$	f_{MAX}		50	30	MHz
Maximum Propagation Delay to Output Clock to Q or $\overline{Q}$	t_{PHL}, t_{PLH}		20	32	ns
Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$	t_{PHL}, t_{PLH}		18	30	ns
Minimum Removal Time, Preset to Clear or Clock	t_{REM}		–	20	ns
Minimum Pulse Width Clock, Preset or Clear	t_W		8	16	ns
Minimum Setup Time Data to Clock	t_S		–	20	ns
Minimum Hold Time Clock to Data	t_H		–3	0	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, C_L = 50pF, t_r = t_f = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	T_A = +25°C	T_A = –40° to +85°C		Unit
			Typ	Guaranteed Limits		
Maximum Clock Frequency	f_{MAX}		–	27	21	MHz
Maximum Propagation Delay from Clock to Q or $\overline{Q}$	t_{PHL}, t_{PLH}		21	35	44	ns
Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$	t_{PHL}, t_{PLH}		21	35	44	ns

AC Electrical Characteristics (Cont'd): (V_{CC} = 5V ±10%, C_L = 50pF $t_r = t_f$ = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions	T_A = +25°C	T_A = −40° to +85°C		Unit
			Typ	Guaranteed Limits		
Minimum Removal Time Preset to Clear or Clock	t_{REM}		–	20	25	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		–	15	19	ns
Maximum Clock Input Rise and Fall Time	t_r, t_f		–	500	500	ns
Minimum Pulse Width Clock, Preset or Clear	t_W		9	16	20	ns
Minimum Setup Time Data to Clock	t_S		–	20	25	ns
Minimum Hold Time Clock to Data	t_H		–3	0	0	ns
Maximum Input Capacitance	C_{IN}		5	10	10	pF
Power Dissipation Capacitance (Per Flip−Flop)	C_{PD}	Note 5	10	–	–	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table:

Inputs				Outputs	
PR	**CLR**	**CLK**	**D**	**Q**	$\overline{\mathbf{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note)	H (Note)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from LOW−to−HIGH
Q_0 = Level of Q before the indicated input conditions were established.
NOTE: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

Pin Connection Diagram