ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4553B
Integrated Circuit
CMOS, 3–Digit BCD Counter
16–Lead DIP Type Package

Description:

The NTE4553B is a 3–digit BCD counter in a 16–Lead DIP type package consisting of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on–chip oscillator provides th low–frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

Features:

- TTL Compatible Outputs
- On–hip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input or Output Voltage (DC or Transient), V_{in}, V_{out} . . . . . –0.5 to V_{DD} + 0.5V
Input Current (DC or Transient) per Pin, I_{in} . . . . . ±10mA
Output Current (DC or Transient) per Pin, I_{out} . . . . . ±20mA
Power Dissipation, P_D 500mW
Derate from +65° to +125°C . . . . . –7.0mW/°C
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C
Lead Temperature (During Soldering, 8 sec max.), T_L . . . . . +260°C

Note 1. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

Electrical Characteristics: (Voltages Referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current	I_{OH}									
(V_{OH} = 4.6Vdc) Source—		5.0	–0.25	–	–0.2	–0.36	–	0.14	–	mAdc
(V_{OH} = 9.5Vdc) Pin3		10	–0.62	–	–0.5	–0.9	–	0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	–1.8	–	–1.5	–3.5	–	1.1	–	mAdc
(V_{OH} = 4.6Vdc) Source—		5.0	–0.65	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 13.5Vdc) Other		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc) Outputs		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
(V_{OL} = 0.4Vdc) Sink	I_{OL}	5.0	0.5	–	0.4	0.88	–	0.28	–	mAdc
(V_{OL} = 0.5Vdc) Pin3		10	1.1	–	0.9	2.25	–	0.65	–	mAdc
(V_{OL} = 1.5Vdc)		15	1.8	–	1.5	8.8	–	1.20	–	mAdc
(V_{OL} = 0.4Vdc) Sink—Other		5.0	3.0	–	2.5	4.0	–	1.6	–	mAdc
(V_{OL} = 0.5Vdc) Outputs		10	6.0	–	5.0	8.0	–	3.5	–	mAdc
(V_{OL} = 1.5Vdc)		15	18	–	15	20	–	10	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.010	5.0	–	150	μAdc
(Per Package)		10	–	10	–	0.020	10	–	300	μAdc
MR = V_{DD}		15	–	20	–	0.030	20	–	600	μAdc
Total Supply Current (Note 3, Note 4) (Dynamic plus Quiescent, Per Package) (C_L = 50pF on All Outputs, All Buffers Switching)	I_T	5.0	I_T = (0.35μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.85μA/kHz) f + I_{DD}							μAdc
		15	I_T = (1.50μA/kHz) f + I_{DD}							μAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\,Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time						
t_{TLH}, t_{THL} = (1.5ns/pF) C_L + 25ns	t_{TLH}, t_{THL}	5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pF) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pF) C_L + 9.5ns		15	–	40	80	ns
Clock to BCD Out	t_{PLH}, t_{PHL}	5.0	–	900	1800	ns
		10	–	500	1000	ns
		15	–	200	400	ns
Clock to Overflow	t_{PHL}	5.0	–	600	1200	ns
		10	–	400	800	ns
		15	–	200	400	ns
Reset to BCD Out	t_{PHL}	5.0	–	900	1800	ns
		10	–	500	1000	ns
		15	–	300	600	ns
Clock to Latch Enable Setup Time	t_{su}	5.0	600	300	–	ns
Master Reset to Latch Enable Setup Time		10	400	200	–	ns
		15	200	100	–	ns
Removal Time	t_{rem}	5.0	–80	–200	–	ns
Latch Enable to Clock		10	–10	–70	–	ns
		15	0	–50	–	ns
Clock Pulse Width	$t_{WH(cl)}$	5.0	550	275	–	ns
		10	200	100	–	ns
		15	150	75	–	ns
Reset Pulse Width	$t_{WH(R)}$	5.0	1200	600	–	ns
		10	600	300	–	ns
		15	450	225	–	ns
Reset Removal Time	t_{rem}	5.0	–80	–180	–	ns
		10	0	–50	–	ns
		15	20	–30	–	ns
Input Clock Frequency	f_{cl}	5.0	–	1.5	0.9	MHz
		10	–	5.0	2.5	MHz
		15	–	7.0	3.5	MHz
Input Clock Rise Time	t_{TLH}	5.0	No Limit			ns
		10				ns
		15				ns
Disable, MR, Latch Enable	t_{TLH}, t_{THL}	5.0	–	–	15	μs
Rise and Fall Times		10	–	–	5.0	μs
		15	–	–	4.0	μs
Scan Oscillator Frequency	1	5.0	–	1.5/C1	–	Hz
(C1 measured in μF)		10	–	4.2/C1	–	Hz
		15	–	7.0/C1	–	Hz

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table:

Inputs				Outputs
Master Reset	Clock	Disable	LE	
0		0	0	No Change
0		0	0	Advance
0	X	1	X	No Change
0	1		0	Advance
0	1		0	No Change
0	0	X	X	No Change
0	X	X		Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

Operating Characteristics:

The NTE4553B three−digit counter consists of three negative edge−triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on−chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. the frequency of the oscillator can be controlled externally by a capacitor between Pin3 and Pin4, or it can be overridden and driven with an external clock at Pin4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable Input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

Pin Connection Diagram