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NTE4551B
Integrated Circuit
CMOS, Quad 2–Channel Analog Multiplexer/Demultiplexer
16–Lead DIP Type Package

Description:

The NTE4551B is a digitally–controlled analog switch in a 16–Lead DIP type package that implements a 4PDT solid state switch with low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

Features:

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range: 3VDC to 18VDC
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3V to 18V (Note: V_{EE} must be ≤ V_{SS})
- Linearized Transfer Characteristics
- Low Noise: $12nV\sqrt{Cycle}$, f ≥1Khz Typ
- Switch Function is Break Before Make

Absolute Maximum Ratings: (Note 1)

DC Supply Voltage Range (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$), V_{DD} . . . . . –0.5V to +18V
Input or Output Voltage (DC or Transient), V_{in}, V_{out}
(Referenced to V_{SS} fo Control Input & V_{EE} for Switch I/O) . . . . . –0.5V to V_{DD} +0.5V
Input Current (Per Control Pin, DC or Transient), I_{in} . . . . . ±10mA
Switch Through Current, I_{sw} . . . . . ±25mA
Power Dissipation (Note 2), P_D 500mW
Derate Above +65°C . . . . . 7mW/°C
Ambient Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum ratings are those values beyond which damage to the device may occur. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for Switch I/O.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

Electrical Characteristics: (Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Supply Requirements (Voltages referenced to V_{EE})										
Power Supply Voltage Range $V_{DD} = -3V \geq V_{SS} \geq V_{EE}$	V_{DD}	–	3	18	3	–	18	3	18	V
Quiescent Current Per Package Control Inputs: $V_{in} = V_{SS}$ or V_{DD} Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500mV$, Note 3	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μA
		10	–	10	–	0.010	10	–	300	μA
		15	–	20	–	0.015	20	–	600	μA
Total Supply Current (Dynamic plus Quiescent, Per Package, $T_A = +25V$ only. The channel component, $(V_{in} - V_{out})/R_{on}$, is not included)	$I_{D(AV)}$	5	(0.07μA/kHz) f + I_{DD}							μA
		10	(0.20μA/kHz) f + I_{DD}							μA
		15	(0.36μA/kHz) f + I_{DD}							μA
Control Input (Voltages referenced to V_{SS})										
Low−Level Input Voltage R_{on} = per spec, I_{off} = per spec	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	V
		10	–	3.0	–	4.50	3.0	–	3.0	V
		15	–	4.0	–	6.75	4.0	–	4.0	V
High−Level Input Voltage R_{on} = per spec, I_{off} = per spec	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	V
		10	7.0	–	7.0	5.50	–	7.0	–	V
		15	11.0	–	11.0	8.25	–	11.0	–	V
Input Leakage Current $V_{in} = 0$ or V_{DD}	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μA
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Switches IN/OUT and Commons OUT/IN – W, X, Y, Z (Voltages referenced to V_{EE})										
Recommended Peak−to−Peak Voltage Into or Out of the Switch (Channel ON or OFF)	$V_{I/O}$	–	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{P-P}
Recommended Static or Dynamic Voltage Across the Switch (Channel ON, Note 3)	ΔV_{switch}	–	0	600	0	–	600	0	300	mV
Output Offset Voltage V_{in} = 0V, No Load	V_{OO}	–	–	–	–	10	–	–	–	μV
ON Resistance $\Delta V_{switch} \leq 500mV$, $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch), Note 3	R_{on}	5.0	–	800	–	250	1050	–	1200	Ω
		10	–	400	–	120	500	–	520	Ω
		15	–	220	–	80	280	–	300	Ω
ΔON Resistance Between any Two Channels in the Same Package	ΔR_{on}	5.0	–	70	–	25	70	–	135	Ω
		10	–	50	–	10	50	–	95	Ω
		15	–	45	–	10	45	–	65	Ω
Off−Channel Leakage Current $V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	I_{off}	15	–	±100	–	±0.05	±100	–	±1000	nA

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. For voltage drops across the switch (ΔV_{switch}) > 600mV (>300mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. he reliability of the device will be unaffected unless the Absolute Maximum ratings are exceeded.

Electrical Characteristics (Cont'd): (Note 2)

Parameter	Symbol	V_{DD} Vdc	–55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Switches IN/OUT and Commons OUT/IN – W, X, Y, Z (Voltages referenced to V_{EE})										
Capacitance, Switch I/O Switch Off	$C_{I/O}$	–	–	–	–	10	–	–	–	pF
Capacitance, Common O/I	$C_{O/I}$	–	–	–	–	17	–	–	–	pF
Capacitance, Feedthrough Channel Off	$C_{I/O}$									
Pins Not Adjacent		–	–	–	–	0.15	–	–	–	pF
Pins Adjacent		–	–	–	–	0.47	–	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	μAdc
		15	–	15	–	0.015	15	–	600	μAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Electrical Characteristics: (C_L = 50pF, T_A = +25°C, $V_{EE} \le V_{SS}$, Note 2)

Parameter	Symbol	$V_{DD}–V_{EE}$ V_{dc}	Min	Typ	Max	Unit
Propagation Delay Times Switch Input to Switch Output t_{PLH}, t_{PHL} = (0.17ns/pF) C_L + 26.5ns, R_L = 10kΩ	t_{PLH}, t_{PHL}	5.0	–	35	90	ns
t_{PLH}, t_{PHL} = (0.08ns/pF) C_L + 11ns, R_L = 10kΩ		10	–	15	40	ns
t_{PLH}, t_{PHL} = (0.06ns/pF) C_L + 9ns, R_L = 10kΩ		15	–	12	30	ns
Control Input to Output R_L = 10kΩ, V_{EE} = V_{SS}	t_{PLH}, t_{PHL}	5.0	–	350	875	ns
		10	–	140	350	ns
		15	–	100	250	ns
Second Harmonic Distortion R_L = 1kΩ, f = 1kHz, V_{in} = $5V_{P–P}$		10	–	0.07	–	%
Bandwidth R_L = 1kΩ, V_{in} = 1/2 $(V_{DD} – V_{EE})_{P–P}$, 20 Log (V_{out}/V_{in}) = –3dB, C_L = 50pF	BW	10	–	17	–	MHz
Off Channel Feedthrough Attenuation R_L = 1kΩ, V_{in} = 1/2 $(V_{DD} – V_{EE})_{P–P}$, f_{in} = 55MHz		10	–	–50	–	dB
Channel Separation R_L = 1kΩ, V_{in} = 1/2 $(V_{DD} – V_{EE})_{P–P}$,, f_{in} = 3MHz		10	–	–50	–	dB
Crosstalk, Control Input to Common O/I R1 = 1Ωk, R_L = 10kΩ, Control t_r = t_f = 20ns		10	–	75	–	mV

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Pin Connection Diagram