ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4547B
Integrated Circuit
CMOS, BCD–to–Seven Segment Decoder/Driver
16–Lead DIP Type Package

Description:

The NTE4547B is a BDC–to seven segment decoder/driver in a 16–Lead DIP type package constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers. The circuit provides the functions of an 8421 BCD–to–seven segment decoder with high output drive capability. Blanking (Bl), can be used to turn off or pulse modulate the brightness of the display. The NTE4547B can drive seven–segment light–emitting diodes (LED), incandescent, fluorescent or gas discharge readouts either directly or indirectly.

Applications include instruments (e.g., counter, DMV, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features:

- High Current Sourcing Outputs (Up to 65mA)
- Low Logic Circuit Power Dissipation
- Supply Voltage Range: +3V to +18V
- Blanking Input
- Readout Blanking on All Illegal Combinations
- Lamp Intensity Modulation Capability
- Multiplexing Capability
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Pin8, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} + 0.5V
Maximum Continuous Output rive Current (Source) per Output, I_{OHmax} 65mA
Maximum Continuous Power Dissipation, P_D 1200mW
Operating Temperature Range, T_A . . . . . –55 to +125°C
Storage Temperature Range, T_{stg} . . . . . –65 to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur. This device contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at Logical 1.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
“1” Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) “0” Level	V_{IL}									
(V_O = 3.8 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 8.8 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.8 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
“1” Level	V_{IH}									
(V_O = 0.5 or 3.8Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 8.8Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.8Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Voltage	V_{OH}									
(I_{OH} = 5mA) Source		5.0	4.0	–	4.2	4.3	–	4.3	–	Vdc
(I_{OH} = 10mA)			–	–	4.1	4.3	–	–	–	Vdc
(I_{OH} = 20mA)			3.8	–	3.9	4.2	–	4.0	–	Vdc
(I_{OH} = 40mA)			–	–	3.7	4.0	–	–	–	Vdc
(I_{OH} = 65mA)			3.1	–	3.2	3.7	–	3.0	–	Vdc
(I_{OH} = 5mA)		10	9.1	–	9.2	9.3	–	9.3	–	Vdc
(I_{OH} = 10mA)			–	–	9.1	9.3	–	–	–	Vdc
(I_{OH} = 20mA)			8.8	–	9.0	9.2	–	9.2	–	Vdc
(I_{OH} = 40mA)			–	–	8.9	9.0	–	–	–	Vdc
(I_{OH} = 65mA)			8.4	–	8.5	8.8	–	8.1	–	Vdc
(I_{OH} = 5mA)		15	14	–	14.2	14.3	–	14.4	–	Vdc
(I_{OH} = 10mA)			–	–	14.1	14.3	–	–	–	Vdc
(I_{OH} = 20mA)			13.8	–	14.0	14.2	–	14.2	–	Vdc
(I_{OH} = 40mA)			–	–	13.8	14.0	–	–	–	Vdc
(I_{OH} = 65mA)			13.5	–	13.5	13.7	–	13.3	–	Vdc
Output Drive Current	I_{OL}									
(V_{OL} = 0.4Vdc) Sink		5.0	0.32	–	0.26	0.44	–	0.18	–	mAdc
(V_{OL} = 0.5Vdc)		10	0.80	–	0.65	1.13	–	0.45	–	mAdc
(V_{OL} = 1.5Vdc)		15	2.10	–	1.7	4.4	–	1.2	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance	C_{in}	–	–	–	–	5.0	7.5	–	–	pF

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both “1” and “0” = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 3.5 \times 10^{-3}(C_L - 50)\, V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Electrical Characteristics (Cont'd): (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Quiescent Current (Per Package) V_{in} = 0 or V_{DD}, I_{out} = 0μA	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	μAdc
		15	–	15	–	0.015	15	–	600	μAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on All Outputs, All Buffers Switching Note 3, Note 5)	I_T	5.0	I_T = (1.9μA/kHz) f + I_{DD}							μAdc
		10	I_T = (3.8μA/kHz) f + I_{DD}							μAdc
		15	I_T = (5.7μA/kHz) f + I_{DD}							μAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 3.5 \times 10^{-3}(C_L - 50)\, V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in volts and f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}	5.0	–	40	80	ns
		10	–	40	80	ns
		15	–	40	80	ns
Output Fall Time	t_{THL}	5.0	–	125	250	ns
		10	–	75	150	ns
		15	–	70	140	ns
Data Propagation Delay Time	t_{PLH}	5.0	–	750	1500	ns
		10	–	300	600	ns
		15	–	200	400	ns
	t_{PHL}	5.0	–	750	1500	ns
		10	–	300	600	ns
		15	–	200	400	ns
Blank Propagation Delay Time	t_{PLH}	5.0	–	750	1500	ns
		10	–	300	600	ns
		15	–	200	400	ns
	t_{PHL}	5.0	–	500	1000	ns
		10	–	250	500	ns
		15	–	170	340	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

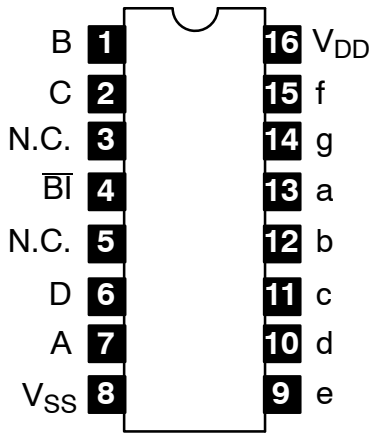
Note 3. The formulas given are for the typical characteristics only at +25°C.

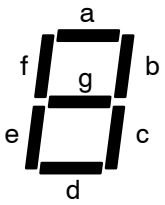
Truth Table:

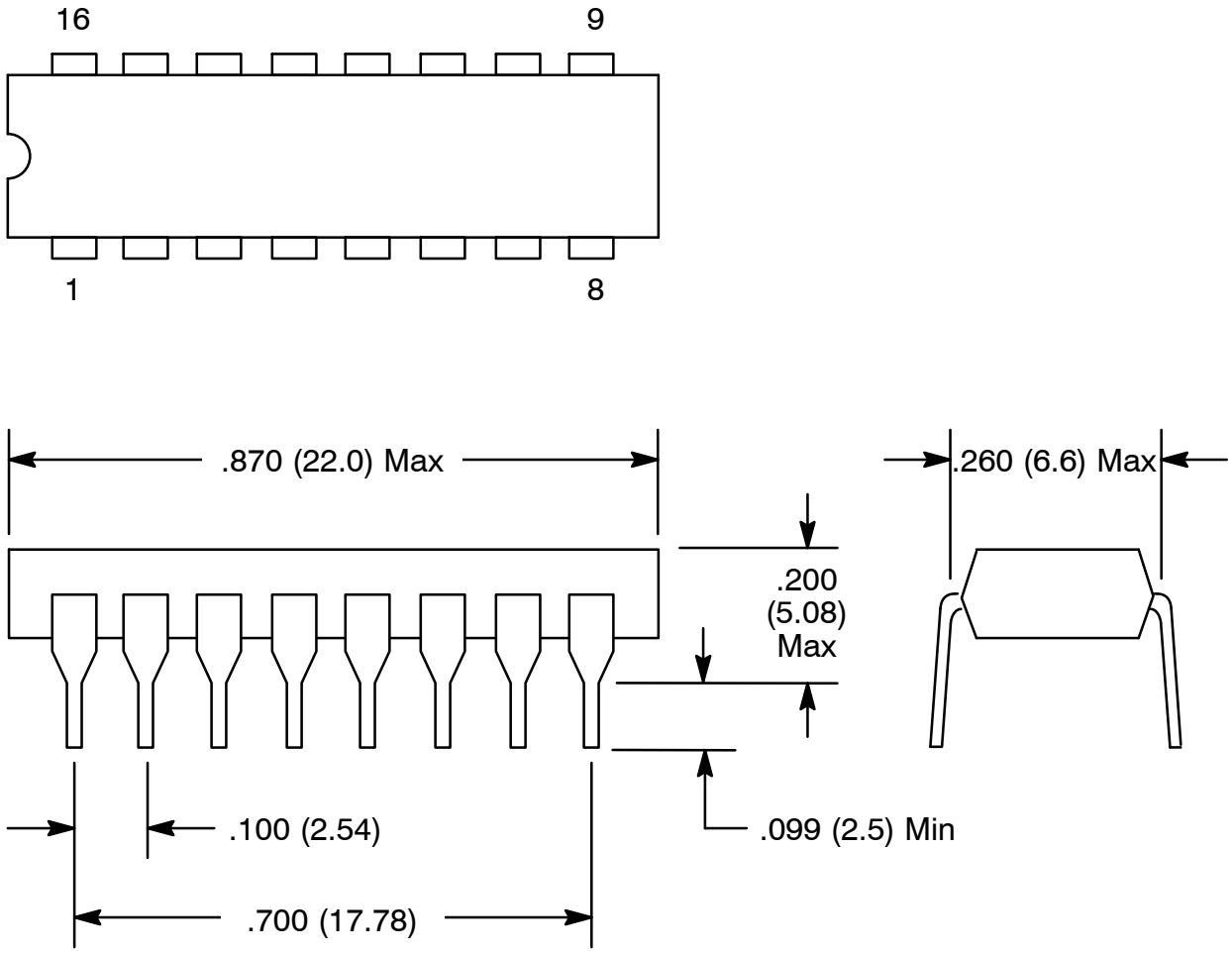
Inputs					Outputs							
$\overline{BI}$	D	C	B	A	a	b	c	d	e	f	g	Display
0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	1	1	0	0	1	3
1	0	1	0	0	0	1	1	0	0	1	1	4
1	0	1	0	1	1	0	1	1	0	1	1	5
1	0	1	1	0	0	0	1	1	1	1	1	6
1	0	1	1	1	1	1	1	0	0	0	0	7
1	1	0	0	0	1	1	1	1	1	1	1	8
1	1	0	0	1	1	1	1	0	0	1	1	9
1	1	0	1	0	0	0	0	0	0	0	0	Blank
1	1	0	1	1	0	0	0	0	0	0	0	Blank
1	1	1	0	0	0	0	0	0	0	0	0	Blank
1	1	1	0	1	0	0	0	0	0	0	0	Blank
1	1	1	1	0	0	0	0	0	0	0	0	Blank
1	1	1	1	1	0	0	0	0	0	0	0	Blank

X = Don't Care

Pin Connection Diagram






16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)