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NTE4527B
Integrated Circuit
CMOS, BCD Rate Multiplier

Description:

The NTE4527B is a BCD rate multiplier (DRM) in a 16–Lead DIP type package that provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This device may b used for arithmetic operations including multiplication and division. Typical applications include digital filters, motor speed control and frequency synthesizers.

Features:

- Quiescent Current = 5nA/Package (Typ) at 5Vdc
- Supply Voltage Range: 3Vdc to 18Vdc
- Low Input Capacitance – 5pF (Typ)
- Internally Synchronized for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and cascade Inputs for cascade Operation of Two or More DRMs
- “9” Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 5)	I_T	5.0	I_T = (0.85µA/kHz) f + I_{DD}							µAdc
		10	I_T = (1.75µA/kHz) f + I_{DD}							µAdc
		15	I_T = (2.6µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 1.2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pF) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pF) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pF) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pF) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pF) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pF) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, Clock to Out	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 115ns		5.0	–	200	400	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 67ns		10	–	100	200	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 45ns		15	–	70	140	ns
Propagation Delay Time, Clock to Out	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 40ns		5.0	–	125	250	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 32ns		10	–	65	130	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 20ns		15	–	45	90	ns
Propagation Delay Time, Clock to E_{out}	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 210ns		5.0	–	295	590	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 97ns		10	–	130	260	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 60ns		15	–	85	170	ns
Propagation Delay Time, Clock to “9”	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 315ns		5.0	–	400	800	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 122ns		10	–	155	310	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 85ns		15	–	110	220	ns
Propagation Delay Time, Set or Clear to Out	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 295ns		5.0	–	380	760	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 132ns		10	–	165	330	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 85ns		15	–	110	220	ns
Propagation Delay Time, Cascade to Out	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 40ns		5.0	–	125	250	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 32ns		10	–	65	130	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 20ns		15	–	45	90	ns
Propagation Delay Time, Strobe to Out	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 145ns		5.0	–	230	260	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 72ns		10	–	105	210	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 45ns		15	–	70	140	ns
Clock Pulse Width	t_{WH}	5.0	500	250	–	ns
		10	200	110	–	ns
		15	150	80	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Clock Pulse Frequency	f_{cl}	5.0	–	2.0	1.2	MHz
		10	–	4.5	2.5	MHz
		15	–	6.0	3.5	MHz
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	–	–	15	μs
		10	–	–	15	μs
		15	–	–	15	μs
Set or Clear Pulse Width	t_{WH}	5.0	240	80	–	ns
		10	100	35	–	ns
		15	75	30	–	ns
Set Removal Time	t_{rem}	5.0	0	–20	–	ns
		10	0	–10	–	ns
		15	0	–7.5	–	ns
Enable In Setup Time	t_{su}	5.0	400	175	–	ns
		10	150	60	–	ns
		15	120	45	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

Inputs										Output Logic Level / Number of Pulses			
D	C	B	A	No. Of Clock Pulses	$\overline{E_{in}}$	STROBE	CASCADE	CLEAR	SET	OUT	$\overline{OUT}$	E_{out}	“9”
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don’t Care

Pin Connection Diagram