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NTE4502B
Integrated Circuit
CMOS, Strobed Hex Inverter/Buffer

Description:

The NTE4502B is a strobed hex buffer/inverter in a 16–Lead DIP type package with 3–state output, an inhibit control, and guaranteed TTL drive over the temperature range. The 3–state output simplifies design by allowing a common bus.

Features:

- Separate Output Disable Control
- 3–State Output
- Output Impedance = 200 Ohms at 5V Supply Guaranteed Over Full Temperature Range
- Input Impedance = 10^{12} Ohms (Typ)
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V

Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V

DC Current Drain, I

Per Input Pin 10mA

Per Output Pin 30mA

Operating Temperature Range, T_A . . . . . –55° to +125°C

Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Note 2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V9in9 and V9out9 be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 4) "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	–0.62	–	–0.5	–0.9	–	–0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	–1.8	–	–1.5	–3.5	–	–1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	3.5	–	2.8	6.6	–	2.0	–	mAdc
(V_{OL} = 0.5Vdc)		10	7.8	–	6.3	17.0	–	4.4	–	mAdc
(V_{OL} = 1.5Vdc)		15	29.0	–	24.0	66.0	–	16.0	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
		10	–	2.0	–	0.004	2.0	–	60	µAdc
		15	–	4.0	–	0.006	4.0	–	120	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 5)	I_T	5.0	I_T = (2.7µA/kHz) f + I_{DD}							µAdc
		10	I_T = (5.3µA/kHz) f + I_{DD}							µAdc
		15	I_T = (8.0µA/kHz) f + I_{DD}							µAdc
Three State Leakage Current	I_{TL}	15	–	±0.1	–	±0.00001	±0.1	–	±3.0	µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 5. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (0.6ns/pf) C_L + 10ns		5.0	–	40	80	ns
t_{THL} = (0.3ns/pf) C_L + 5.0ns		10	–	20	40	ns
t_{THL} = (0.27ns/pf) C_L + 1.5ns		15	–	15	30	ns
Propagation Delay Time, Data to Q	t_{PHL}	5.0	–	135	270	ns
		10	–	55	110	ns
		15	–	40	80	ns
Propagation Delay Time, Inhibit to Q	t_{PHL}	5.0	–	335	670	ns
		10	–	145	290	ns
		15	–	95	190	ns
Propagation Delay Time, Data to Q, Inhibit to Q	t_{PLH}	5.0	–	295	590	ns
		10	–	130	260	ns
		15	–	95	190	ns
3−State Propagation Delay, Output “1” to High Impedance	t_{PHZ}	5.0	–	65	130	ns
		10	–	30	60	ns
		15	–	25	50	ns
3−State Propagation Delay, High Impedance to Output “1”	t_{PZH}	5.0	–	260	520	ns
		10	–	105	210	ns
		15	–	80	160	ns
3−State Propagation Delay, Output “0” to High Impedance	t_{PLZ}	5.0	–	65	130	ns
		10	–	30	60	ns
		15	–	25	50	ns
3−State Propagation Delay, High Impedance to Output “0”	t_{PZL}	5.0	–	260	520	ns
		10	–	105	210	ns
		15	–	80	160	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don’t Care

Pin Connection Diagram