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NTE4089B
Integrated Circuit
CMOS, Binary Rate Multiplier

Description:

The NTE4089B is a low–power 4–bit digital rate multiplier in a 16–Lead DIP type package that provides an output pulse rate that is the clock–input–pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses. This device may be used in conjunction with an up/down counter and control logic used to perform arithmetic operations (adds, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigometric functions, A/D and D/A conversions, and frequency division.

For words of more than 4–bits, NTE4089B devices may be cascaded in two different modes: an Add mode and a Multiply mode. In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

In the Multiply mode the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second multiplier. Thus, the output rate will be

$$\frac{11}{16} \times \frac{13}{16} = \frac{143}{256}$$

Features:

- Cascadable to Multiples of 4–Bits
- Set to “15” Input and “15” Detect Output
- 5V, 10V, and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package Temperature Range)
  = 1V at V_{DD} = 5V
  = 2V at V_{DD} = 10V
  = 2.5V at V_{DD} = 15V

Applications:

- Numerical Control
- Instrumentation
- Digital Filtering
- Frequency Synthesis

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages referenced to V_{SS} terminal), V_{DD} ..... −0.5 to +20V
Input Voltage Range, All Inputs ..... −0.5 to V_{DD}+0.5V
DC Input Current, Any One Input ..... ±10mA
Power Dissipation (T_A = −55° to +100°C), P_D 500mW
T_A = +100° to +125°C ..... Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A ..... −55° to +125°C
Storage Temperature Range, T_{stg} ..... −65° to +150°C
Lead Temperature (During Soldering, 1/16" ±1/32" from case, 10sec Max), T_L ..... +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Min	Typ	Max	Unit
Supply Voltage Range (For T_A = Full package Temperature)	3	–	18	V
Set or Clear Pulse Width, t_W				
V_{DD} = 5V	160	–	–	ns
V_{DD} = 10V	90	–	–	ns
V_{DD} = 15V	60	–	–	ns
Clock Pulse Width, t_W				
V_{DD} = 5V	330	–	–	ns
V_{DD} = 10V	170	–	–	ns
V_{DD} = 15V	100	–	–	ns
Clock Frequency, f_{CL}				
V_{DD} = 5V	dc	–	1.2	MHz
V_{DD} = 10V	dc	–	2.5	MHz
V_{DD} = 15V	dc	–	3.5	MHz
Clock Rise or Fall Time (All Voltages), t_{rCL}, t_{fCL}	–	–	15	µs
Inhibit In Setup Time, t_{SU}				
V_{DD} = 5V	100	–	–	ns
V_{DD} = 10V	40	–	–	ns
V_{DD} = 15V	20	–	–	ns
Inhibit In Removal Time, t_{REM}				
V_{DD} = 5V	240	–	–	ns
V_{DD} = 10V	130	–	–	ns
V_{DD} = 15V	110	–	–	ns
Set Removal Time, t_{REM}				
V_{DD} = 5V	150	–	–	ns
V_{DD} = 10V	80	–	–	ns
V_{DD} = 15V	50	–	–	ns
Clear Removal Time, t_{REM}				
V_{DD} = 5V	60	–	–	ns
V_{DD} = 10V	40	–	–	ns
V_{DD} = 15V	30	–	–	ns

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	µA
	–	0,15	15	20	20	600	600	–	0.04	20	µA
	–	0,20	20	100	100	3000	3000	–	0.08	100	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input High Voltage V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$±10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time Clock to $\overline{Out}$	t_{PHL}, t_{PLH}	V_{DD} = 5V	–	110	220	ns
		V_{DD} = 10V	–	55	110	ns
		V_{DD} = 15V	–	45	90	ns
Clock or Strobe to Out		V_{DD} = 5V	–	150	300	ns
		V_{DD} = 10V	–	75	150	ns
		V_{DD} = 15V	–	60	120	ns
Clock or Inhibit Out High Level to Low Level		V_{DD} = 5V	–	360	720	ns
		V_{DD} = 10V	–	160	320	ns
		V_{DD} = 15V	–	110	220	ns

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level to Low Level		V_{DD} = 5V	–	250	500	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	75	150	ns
Clear to Out		V_{DD} = 5V	–	380	760	ns
		V_{DD} = 10V	–	175	350	ns
		V_{DD} = 15V	–	130	260	ns
Clock to "9" or "15" Out		V_{DD} = 5V	–	300	600	ns
		V_{DD} = 10V	–	125	250	ns
		V_{DD} = 15V	–	90	180	ns
Cascade to Out		V_{DD} = 5V	–	90	180	ns
		V_{DD} = 10V	–	45	90	ns
		V_{DD} = 15V	–	35	70	ns
Inhibit In to Inhibit Out		V_{DD} = 5V	–	160	320	ns
		V_{DD} = 10V	–	75	150	ns
		V_{DD} = 15V	–	55	110	ns
Set to Out		V_{DD} = 5V	–	330	660	ns
		V_{DD} = 10V	–	150	300	ns
		V_{DD} = 15V	–	110	220	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Maximum Clock Frequency	f_{CL}	V_{DD} = 5V	1.2	2.4	–	MHz
		V_{DD} = 10V	2.5	5.0	–	MHz
		V_{DD} = 15V	3.5	7.0	–	MHz
Minimum Clock Pulse Width	t_W	V_{DD} = 5V	–	165	330	ns
		V_{DD} = 10V	–	85	170	ns
		V_{DD} = 15V	–	50	100	ns
Clock Rise or Fall Time	t_{rCL}, t_{fCL}	V_{DD} = 5V	–	–	15	µs
		V_{DD} = 10V	–	–	15	µs
		V_{DD} = 15V	–	–	15	µs
Minimum Set or Clear Pulse Width	t_W	V_{DD} = 5V	–	80	160	ns
		V_{DD} = 10V	–	45	90	ns
		V_{DD} = 15V	–	30	60	ns
Minimum Inhibit–In Setup Time	t_{SU}	V_{DD} = 5V	–	50	100	ns
		V_{DD} = 10V	–	20	40	ns
		V_{DD} = 15V	–	10	20	ns

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Inhibit–In Removal Time	t_{REM}	V_{DD} = 5V	–	120	240	ns
		V_{DD} = 10V	–	65	130	ns
		V_{DD} = 15V	–	55	110	ns
Minimum Set Removal Time	t_{REM}	V_{DD} = 5V	–	75	150	ns
		V_{DD} = 10V	–	40	80	ns
		V_{DD} = 15V	–	25	50	ns
Minimum Clear Removal Time	t_{REM}	V_{DD} = 5V	–	30	60	ns
		V_{DD} = 10V	–	20	40	ns
		V_{DD} = 15V	–	15	30	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Truth Table:

Inputs										Outputs			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	#	#	H	#
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	X	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

Depends on internal state of counter.

Pin Connection Diagram