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NTE4086B
Integrated Circuit
CMOS, Expandable 4–Wide, 2–Input AND/OR Invert Gate

Description:

The NTE4086B is supplied in a 14–Lead DIP type package and contains one 4–wide, 2–input AND–OR–INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4–wide A–O–I function INHIBIT/$\overline{EXP}$ is tied to V_{SS} and ENABLE/EXP to V_{DD}.

Features:

- Medium–Speed Operation: t_{PHL} = 90ns; t_{PLH} = 140ns (Typ) at 10V
- INHIBIT and ENABLE Inputs
- Buffered Outputs
- Maximum Input Current of 1μA at 18V over Full Package Temperature Range; 100nA at 18V and +25°C
- Noise Margin (Full Package Temperature Range)
  = 1V at V_{DD} = 5V
  = 2V at V_{DD} = 10V
  = 2.5V at V_{DD} = 15V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages referenced to V_{SS} terminal), V_{DD} . . . . . −0.5 to +20V
Input Voltage Range, All Inputs . . . . . −0.5 to V_{DD}+0.5V
DC Input Current, Any One Input . . . . . ±10mA
Power Dissipation (T_A = −55° to +100°C), P_D 500mW
T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 1/16” ±1/32” from case, 10sec Max), T_L . . . . . +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Min	Typ	Max	Unit
Supply Voltage Range (For T_A = Full package Temperature)	3	–	18	V

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

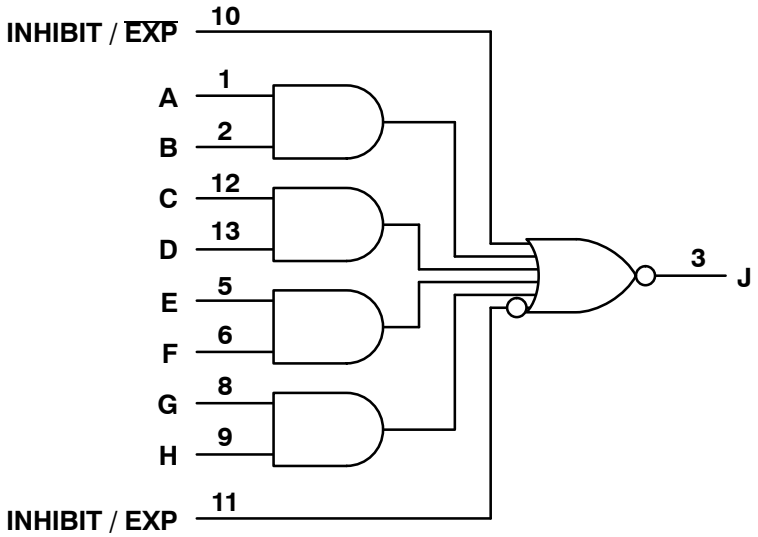
Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	µA
	–	0,15	15	4	4	120	120	–	0.02	4	µA
	–	0,20	20	20	20	600	600	–	0.04	20	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input High Voltage V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm 10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics: (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (Data) High−to−Low Level	t_{PHL}	V_{DD} = 5V	–	225	450	ns
		V_{DD} = 10V	–	90	180	ns
		V_{DD} = 15V	–	60	120	ns
Low−to−High Level	t_{PLH}	V_{DD} = 5V	–	310	620	ns
		V_{DD} = 10V	–	125	250	ns
		V_{DD} = 15V	–	90	180	ns
Propagation Delay Time (Inhibit) High−to−Low Level	t_{PHL}	V_{DD} = 5V	–	150	300	ns
		V_{DD} = 10V	–	60	120	ns
		V_{DD} = 15V	–	40	80	ns
Low−to−High Level	t_{PLH}	V_{DD} = 5V	–	250	500	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	70	140	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Functional Diagram



J = INH + $\overline{\text{ENABLE}}$ + AB + CD + EF + GH
Logic 1 = HIGH
Logic 0 = LOW

V_{DD} = Pin14
V_{SS} = Pin7
N.C. = Pin4

Pin Connection Diagram