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NTE4085B Integrated Circuit CMOS, Dual 2-Wide, 2-Input AND/OR Invert Gate

Description:

The NTE4085B is supplied in a 14-Lead DIP type package and contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

Features:

- Medium-Speed Operation: $t_{PHL} = 90ns$; $t_{PLH} = 125ns$ (Typ) at 10V
- Individual Inhibit Controls
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of $1\mu A$ at 18V over Full Package Temperature Range; 100nA at 18V and $+25^{\circ}C$
- Noise Margin (Full Package Temperature Range)
 - = 1V at $V_{DD} = 5V$
 - = 2V at $V_{DD} = 10V$
 - = 2.5V at $V_{DD} = 15V$
- 5V, 10V, and 15V Parametric Ratings

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages referenced to V_{SS} terminal), V_{DD} -0.5 to +20V
 Input Voltage Range, All Inputs -0.5 to $V_{DD}+0.5V$
 DC Input Current, Any One Input $\pm 10mA$
 Power Dissipation ($T_A = -55^{\circ}$ to $+100^{\circ}C$), P_D 500mW
 $T_A = +100^{\circ}$ to $+125^{\circ}C$ Derate Linearly at 12mW/ $^{\circ}C$ to 200mW
 Device Dissipation (Per Output Transistor)
 For $T_A =$ Full Package Temperature Range 100mW
 Operating Temperature Range, T_A -55° to $+125^{\circ}C$
 Storage Temperature Range, T_{stg} -65° to $+150^{\circ}C$
 Lead Temperature (During Soldering, $1/16'' \pm 1/32''$ from case, 10sec Max), T_L $+265^{\circ}C$

Recommended Operating Conditions: (Note 1)

Parameter	Min	Typ	Max	Unit
Supply Voltage Range (For $T_A =$ Full package Temperature)	3	-	18	V

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

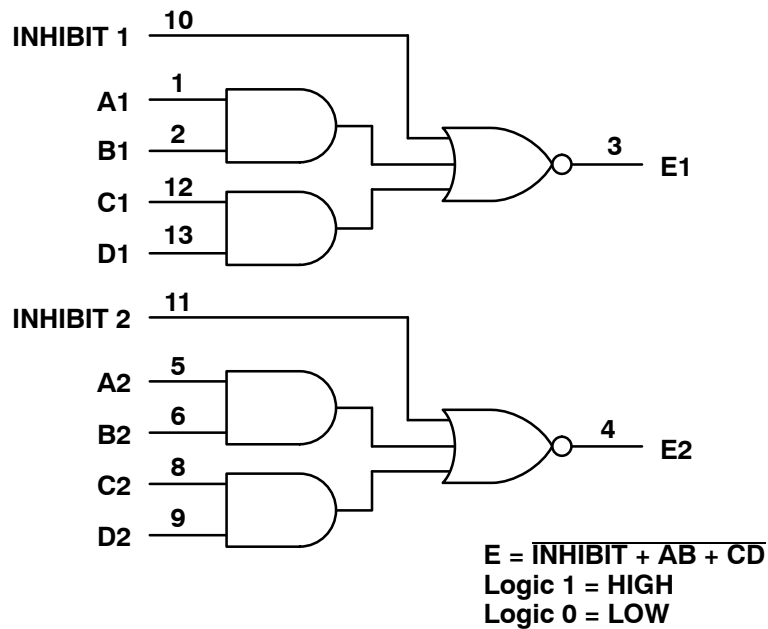
Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55°C	-40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I _{DD} Max.	-	0,5	5	1	1	30	30	-	0.02	1	μA
	-	0,10	10	2	2	60	60	-	0.02	2	μA
	-	0,15	15	4	4	120	120	-	0.02	4	μA
	-	0,20	20	20	20	600	600	-	0.04	20	μA
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	-	mA
Output High (Source) Current I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1.0	-	mA
	2.5	0,5	5	-2.0	-1.8	-1.3	-1.15	-1.6	-3.2	-	mA
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	mA
	13.5	0,15	15	-4.2	-4.0	-2.8	-2.4	-3.4	-6.8	-	mA
Output Voltage Low-Level V _{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	V
	-	0,15	15	0.05				-	0	0.05	V
Output Voltage High-Level V _{OH} Min.	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	V
	-	0,15	15	14.95				14.95	15	-	V
Input Low Voltage V _{IL} Max.	0.5,4.5	-	5	1.5				-	-	1.5	V
	1,9	-	10	3.0				-	-	3.0	V
	1.5,13.5	-	15	4.0				-	-	4.0	V
Input High Voltage V _{IH} Min.	0.5,4.5	-	5	3.5				3.5	-	-	V
	1,9	-	10	7.0				7.0	-	-	V
	1.5,13.5	-	15	11.0				11.0	-	-	V
Input Current, I _{IN} Max.	-	0,18	18	±0.1	±0.1	±1.0	±1.0	-	±10 ⁻⁵	±0.1	μA

Dynamic Electrical Characteristics: ($T_A = +25^\circ\text{C}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$, t_r and $t_f = 20\text{ns}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time (Data) High-to-Low Level	t_{PHL}	$V_{\text{DD}} = 5\text{V}$	–	225	450	ns
		$V_{\text{DD}} = 10\text{V}$	–	90	180	ns
		$V_{\text{DD}} = 15\text{V}$	–	65	130	ns
Low-to-High Level	t_{PLH}	$V_{\text{DD}} = 5\text{V}$	–	310	620	ns
		$V_{\text{DD}} = 10\text{V}$	–	125	250	ns
		$V_{\text{DD}} = 15\text{V}$	–	90	180	ns
Propagation Delay Time (Inhibit) High-to-Low Level	t_{PHL}	$V_{\text{DD}} = 5\text{V}$	–	150	300	ns
		$V_{\text{DD}} = 10\text{V}$	–	60	120	ns
		$V_{\text{DD}} = 15\text{V}$	–	40	80	ns
Low-to-High Level	t_{PLH}	$V_{\text{DD}} = 5\text{V}$	–	250	500	ns
		$V_{\text{DD}} = 10\text{V}$	–	100	200	ns
		$V_{\text{DD}} = 15\text{V}$	–	70	140	ns
Transition Time	t_{THL} or t_{TLH}	$V_{\text{DD}} = 5\text{V}$	–	100	200	ns
		$V_{\text{DD}} = 10\text{V}$	–	50	100	ns
		$V_{\text{DD}} = 15\text{V}$	–	40	80	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Functional Diagram



$V_{\text{DD}} = \text{Pin14}$
 $V_{\text{SS}} = \text{Pin7}$

Pin Connection Diagram

