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NTE4048B
Integrated Circuit
CMOS, Multifunction Expandable 8–Input Gate

Description:

The NTE4048B is an 8–input gate in a 16–Lead DIP type package having four control inputs. Three binary control inputs — K_a, K_b, and K_c — provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR.

A fourth control input, K_d, provides the user with a 3–state output. When control input K_d is high, the output is either a logic “1” or a logic “0” depending on the inner states. When control input K_d is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs into an NTE4048B. For example, two NTE4048Bs can be cascaded to provide a 16–input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

Features:

- Three–State Output
- Many Logic Functions Available in One Package
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V (Full Package Temperature Range), 100nA at 19V and +25°C
- Noise Margin (Full Package Temperature Range) = 1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V
- 5V, 10V, and 15V Parametric Ratings

Applications:

- Selection of up to 8 Logic Functions
- Digital Control of Logic
- General Purpose Gating Logic
  - Decoding
  - Encoding

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages referenced to V_{SS} terminal), V_{DD} . . . . . −0.5 to +20V
Input Voltage Range, All Inputs . . . . . −0.5 to V_{DD}+0.5V
DC Input Current, Any One Input . . . . . ±10mA
Power Dissipation (T_A = −55° to +100°C), P_D 500mW
T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 1/16” ±1/32” from case, 10sec Max), T_L . . . . . +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Min	Typ	Max	Unit
Supply Voltage Range (For T_A = Full package Temperature)	3	–	18	V

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	µA
	–	0,15	15	1.0	1.0	30	30	–	0.01	1.0	µA
	–	0,20	20	5.0	5.0	150	150	–	0.02	5.0	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input High Voltage V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm10^{-5}$	±0.1	µA
3–State Output Current I_{OUT}	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	µA

Dynamic Electrical Characteristics: (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time Inputs to Output and K_a to Output	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	300	600	ns
		V_{DD} = 10V	–	150	300	ns
		V_{DD} = 15V	–	120	240	ns
K_b to Output		V_{DD} = 5V	–	225	450	ns
		V_{DD} = 10V	–	85	170	ns
		V_{DD} = 15V	–	55	110	ns
K_c to Output		V_{DD} = 5V	–	140	280	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Expand Input to Output		V_{DD} = 5V	–	190	380	ns
		V_{DD} = 10V	–	90	180	ns
		V_{DD} = 15V	–	65	130	ns
3−State Propagation Delay (R_L = 1kΩ) K_d to Output	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	V_{DD} = 5V	–	80	160	ns
		V_{DD} = 10V	–	35	70	ns
		V_{DD} = 15V	–	25	50	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.0	pF
3−State Output Capacitance			–	5.0	10.0	pF

Implementation of Expand Input for 9 or More Inputs:

Output Function	Function Needed at Expand Input	Output Boolean Expression
NOR	OR	$J = \overline{(A + B + C + D + E + F + G + H)} + (EXP)$
OR	OR	$J = (A + B + C + D + E + F + G + H) + (EXP)$
AND	NAND	$J = (ABCDEFGH) \bullet \overline{(EXP)}$
NAND	NAND	$J = \overline{(ABCDEFGH) \bullet \overline{(EXP)}}$
OR / AND	NOR	$J = (A + B + C + D) \bullet (E + F + G + H) \bullet \overline{(EXP)}$
OR / NAND	NOR	$J = \overline{(A + B + C + D) \bullet (E + F + G + H) \bullet \overline{(EXP)}}$
AND / NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND / OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note 2. (EXP) designates the EXPAND function (i.e., $X_1 + X_2 + \ldots X_N$).
Note 3. Refer to “Function Truth Table” for connection of unused inputs.

Function Truth Table:

Output Function	Boolean Expression	K_a	K_b	K_c	Unused Input
NOR	$J = \overline{A + B + C + D + E + F + G + H}$	0	0	0	V_{SS}
OR	$J = A + B + C + D + E + F + G + H$	0	0	1	V_{SS}
OR / AND	$J = (A + B + C + D) \bullet (E + F + G + H)$	0	1	0	V_{SS}
OR / NAND	$J = \overline{(A + B + C + D) \bullet (E + F + G + H)}$	0	1	1	V_{SS}
AND	$J = ABCDEFGH$	1	0	0	V_{DD}
NAND	$J = \overline{ABCDEFGH}$	1	0	1	V_{DD}
AND / NOR	$J = \overline{ABCD + EFGH}$	1	1	0	V_{DD}
AND / OR	$J = ABCD + EFGH$	1	1	1	V_{DD}
$K_d = 1$ Normal Inverter Action					
$K_d = 0$ High Impedeance Output					

EXPAND Input = 0

Pin Connection Diagram