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NTE4035B
Integrated Circuit
CMOS, 4–Bit Parallel–In/Parallel–Out Shift Register

Description:

The NTE4035B is a 4–bit shift register in a 16–Lead DIP type package constructed with MOS P–Channel an N–Channel enhancement mode devices in a single monolithic structure. It consists of a 4–stage clocked serial–shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial–right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip–flop stages. J–K logic forms the serial input to the first stage. With the J and K inputs connected together they operate as a serial “D” input.

Features:

- 4–Stage Clocked Serial–Shift Operation
- Synchronous Parallel Loading of All Four Stages
- J–K Serial Inputs on First Stage
- Asynchronous True/Complement Control of All Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive–Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of riving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . −0.5 to +18.0V
Input Voltage (DC or Transient), V_{IN} . . . . . −0.5 to V_{DD} +0.5V
Output Voltage (DC or Transient), V_{OUT} . . . . . −0.5 to V_{DD} +0.5V
Input Current (DC or Transient, Per Pin), I_{IN} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{OUT} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . −7.0mW/°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 10sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs all buffers switching, Note 3, Note 4)	I_T	5.0	I_T = (1.0µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.0µA/kHz) f + I_{DD}							µAdc
		15	I_T = (3.0µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns	t_{TLH}, t_{THL}	5	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 12.5ns		15	–	40	80	ns
Propagation Delay Time, Clock or Reset to Q t_{PLH}, t_{PHL} = (1.75ns/pf) C_L + 223ns	t_{PLH}. t_{PHL}	5	–	300	600	ns
t_{PLH}, t_{PHL} = (0.70ns/pf) C_L + 89ns		10	–	130	260	ns
t_{PLH}, t_{PHL} = (0.53ns/pf) C_L + 67ns		15	–	95	190	ns
Clock Pulse Width	t_{WH}	5	335	135	–	ns
		10	165	45	–	ns
		15	125	40	–	ns
Reset Pulse Width	t_{WH}	5	400	80	–	ns
		10	175	40	–	ns
		15	130	35	–	ns
Reset Removal Time	t_{rem}	5	80	40	–	ns
		10	30	15	–	ns
		15	25	10	–	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5	No Limit			–
		10				–
		15				–
Clock Pulse Frequency	f_{cl}	5	–	2.5	1.2	MHz
		10	–	6.0	2.0	MHz
		15	–	10.0	3.0	MHz
J–$\overline{K}$ to Clock Setup Time	t_{su}	5	500	120	–	ns
		10	200	50	–	ns
		15	150	30	–	ns
Clock to J–$\overline{K}$ Hold Time	t_h	5	40	–40	–	ns
		10	30	–5	–	ns
		15	25	0	–	ns
P/S to Clock Setup Time	t_{su}	5	500	25	–	ns
		10	200	10	–	ns
		15	150	7.5	–	ns
Clock to P/S Hold Time	t_h	5	30	–70	–	ns
		10	20	–20	–	ns
		15	20	–10	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Switching Characteristics (Cont'd): (C_L = 50pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
D_P to Clock Setup Time	t_{su}	5	500	90	–	ns
		10	200	20	–	ns
		15	150	15	–	ns
Clock to D_P Hold Time	t_h	5	90	–25	–	ns
		10	40	0	–	ns
		15	40	5	–	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

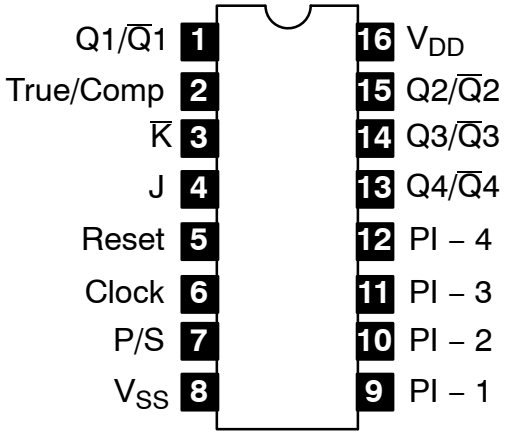
Note 3. The formulas given are for the typical characteristics only at +25°C.

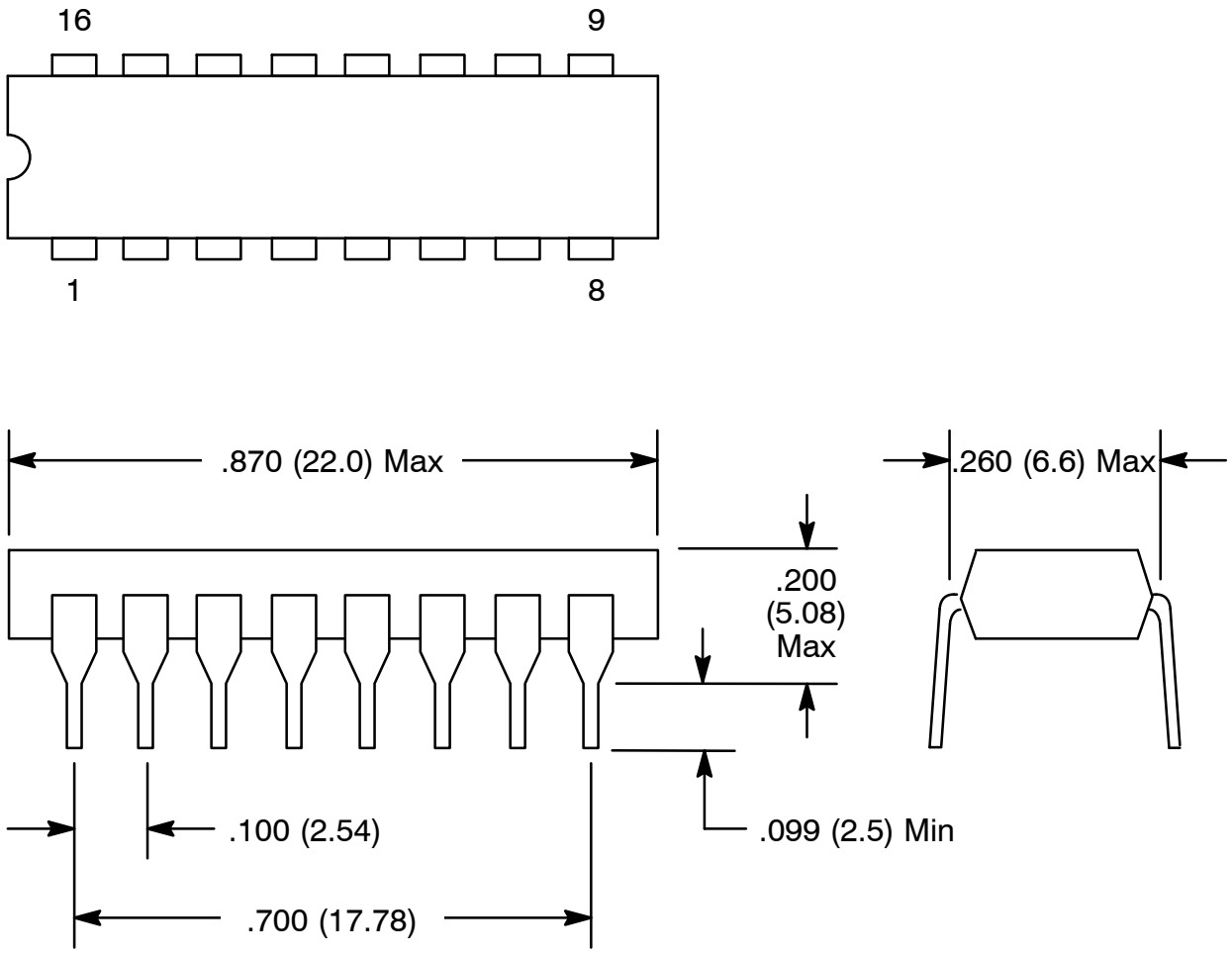
Truth Table

Inputs				t_n Output Q_0
C	J	$\overline{K}$	R	
⎍	0	0	0	0
⎍	0	1	0	Q0 (n – 1)
⎍	1	0	0	$\overline{Q0}$ (n – 1)
⎍	1	1	0	1
⎎	X	X	0	Q0 (n – 1)
X	X	X	1	0

X = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6) Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)