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NTE4031B
Integrated Circuit
CMOS, 64–Stage Static Shift Register

Description:

The NTE4031B is an integrated, complementary MOS, 64–stage, fully static shift register in a 16–Lead DIP type package. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into th first stage of the register and is shifted one stage at each positive transition of th CLOCK.

Data output is available in both true and complement forms from the 64^{th} stage. Both the DATA OUT (Q) and $\overline{\text{DATA OUT}}$ ($\overline{Q}$) outputs are fully buffered.

The CLOCK input of the NTE4031B is fully buffered, and presents only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan–out and transition time requirements when cascading packages.

Features:

- Wide Supply Voltage Range: 3Vdc to 18Vdc
- High Noise Immuntity: 0.45 V_{DD} (Typ)
- Low Power TTL Compatibility: Fan Out of 2 Driving 74L or 1 Driving 74LS
- Fully Static Opration: DC to 8Mhz, V_{DD} = 10V (Typ)
- Fully Buffered Clock Input: 5pF (Typ) Input Capacitance
- Single Phase Clocking Requirements
- Fully Buffered Outputs
- High Current Sinking Capability: 1.6mA at V_{DD} = 5V and +25°C
- Q Output

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage, V_{IN} . . . . . –0.5 to V_{DD} +0.5V
Power Dissipation, P_D 500mW
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec max), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of “Recommended Operating Conditions” and “Electrical Characteristics” provide conditions fo actual device operation.

Recommended Operating Conditions: (Voltages referenced to V_{SS})

Supply Voltage, V_{DD} . . . . . 3 to 15V

Input Voltage, V_{IN} . . . . . 0 to V_{DD} V

Operating Temperature Range, T_A . . . . . −55° to +125°C

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Quiescent Device Current $V_{IN} = V_{DD}$ or V_{SS}	I_{DD}	5.0	–	5.0	–	0.01	5.0	–	150	µAdc
		10	–	10	–	0.01	10	–	300	µAdc
		15	–	20	–	0.02	20	–	600	µAdc
Low Level Output Voltage	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{IH} = V_{DD}$, $V_{IL} = 0$, $\|I_O\| < 1\mu A$		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
High Level Output Voltage	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{IH} = V_{DD}$, $V_{IL} = 0$, $\|I_O\| < 1\mu A$		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Low Level Input Voltage ($\|I_O\| < 1\mu A$)	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
High Level Input Voltage ($\|I_O\| < 1\mu A$)	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
High Level Output Drive Current (All Outputs, Note 2)	I_{OH}									
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Low Level Output Drive Current (Q Output, Note 2)	I_{OL}									
(V_{OH} = 0.4Vdc)		5.0	2.3	–	1.9	3.8	–	1.3	–	mAdc
(V_{OH} = 0.5Vdc)		10	5.1	–	4.2	8.4	–	2.6	–	mAdc
(V_{OH} = 1.5Vdc)		15	10.5	–	8.8	17	–	6.1	–	mAdc
($\overline{Q}$ and CL_D Outputs, Note 2)										
(V_{OH} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OH} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OH} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{IN}	15	–	±0.1	–	$\pm 10^{-5}$	±0.1	–	±0.1	µAdc

Note 2. I_{OH} and I_{OL} are tested one output at a time.

Switching Characteristics: (C_L = 50pF, $t_r = t_f$ = 20ns, R_L = 200k, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Propagation Delay Time Clock to Q and $\overline{Q}$	t_{PLH}, t_{PHL}	5.0	–	300	600	ns
		10	–	125	250	ns
		15	–	100	200	ns
Clock to CL_D		5.0	–	125	250	ns
		10	–	60	125	ns
		15	–	50	100	ns
Output Transition Time, All Outputs	t_{TLH}, t_{THL}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Minimum Data Setup Time DATA IN or RECIRCULATE IN to Clock	t_{SU_0}, t_{SU_1}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Minimum Data Hold Time Clock to DATA IN or RECIRCULATE IN	t_{H_0}, t_{H_1}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Minimum Clock Pulse Width	t_{WL}, t_{WH}	5.0	–	150	30	ns
		10	–	60	125	ns
		15	–	50	100	ns
Maximum Clock Frequency	f_{CL}	5.0	1.6	3.2	–	MHz
		10	4.0	8.0	–	MHz
		15	5.0	10.0	–	MHz
Maximum Clock Input Rise and Fall Times (Note 4)	t_{RCL}, t_{FCL}	5.0	15	–	–	ns
		10	10	–	–	ns
		15	5	–	–	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Note 3. AC Parameters are guaranteed by DC correlated testing.

Note 4. When clocking cascaded packages in parallel, one should insure that: $t_{rCL} \leq 2\ (t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

Truth Tables:

Mode Control (Data Selection)

Mode Control	Data In	Recirculate In	Data Input First Stage
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

X = Don't Care

Truth Tables (Cont'd):

Each Stage

D_S	Clock	Q_n
0	⎍	0
1	⎍	1
X	⎎	NC

X = Don't Care
NC = No Change

Pin Connection Diagram