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NTE4030B
Integrated Circuit
CMOS, Quad Exclusive OR Gate
14–Lead DIP Type Package

Description:

The NTE4030B consists of four independent Exclusive–OR gates in a 14–Lead DIP type package and provides the system designer with a means for direct implementation of the Exclusive–OR function.

Features:

- Medium–Speed Operation: t_{PHL}, t_{PLH} = 65ns (Typ) at V_{DD} = 10V, C_L = 50pF
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Maximum Input Current of 1μA at 18V over Full Package Temperature Range: 100nA at 18V and +25°C
- Noise Margin (over Full Package Temperature Range):
  1.0V at V_{DD} = 5V
  2.0V at V_{DD} = 10V
  2.5V at V_{DD} = 15V

Applications:

- Even and Odd–Parity Generators and Checkers
- Logical Comparators
- Adders/Subtractors
- General Logic Functions

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage Range (Voltages referenced to V_{SS}), V_{DD} . . . . . –0.5 to +20.0V
Input Voltage Range (All Inputs) . . . . . –0.5 to V_{DD} +0.5V
DC Input Current (Any One Input) . . . . . ±10mA
Power Dissipation (Per Package), P_D
For T_A = –55° to +100°C 500mW
For T_A = +100° to +125°C . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec max), T_L . . . . . +265°C

Recommended Operating Conditions:

DC Supply Voltage (For T_A = Full Package Temperature Range) . . . . . 3 to 18V

Static Electrical Characteristics:

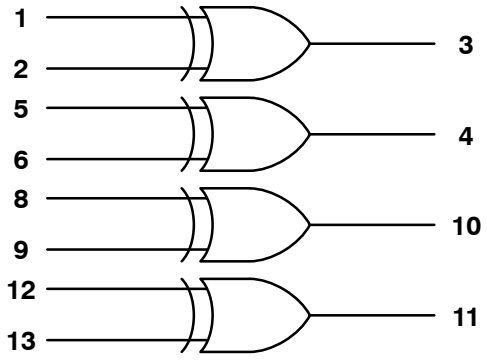
Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	µA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	µA
	–	0,15	15	1.0	1.0	30	30	–	0.01	1.0	µA
	–	0,20	20	5.0	5.0	150	150	–	0.02	5.0	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA
Output Voltage Low–Level V_{OL} Max.	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	V
	–	15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	5	5	4.95				4.95	5	–	V
	–	10	10	9.95				9.95	10	–	V
	–	15	15	14.95				14.95	15	–	V
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input High Voltage V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	V
	1,9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm 10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time from	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	140	280	ns
		V_{DD} = 10V	–	65	130	ns
		V_{DD} = 15V	–	50	100	ns
Transition Time	t_{THL} or t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Logic Diagram



V_{DD} = Pin14
V_{SS} = Pin7

Pin Connection Diagram