ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE40194B
Integrated Circuit
CMOS, 4–Bit Bidirectional Universal Shift Register

Description:

The NTE40194B is a universal shift register in a 16–Lead DIP type package featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, an a direct overriding clear input. In the parallel–load mode (S0 and S1 are high), dat is loaded into the associated flip–flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the $\overline{\text{RESET}}$ input resets all stages and forces all outputs low.

Features:

- Medium–Speed Operation: f_{CL} = 12Mhz (TYP) at V_{DD} = 10V
- Full Static Operation
- Synchronous Parallel or Serial Operation
- Asynchronous Master Reset
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings

Applications:

- Arithmetic Unit Bus Registers
- Serial/Parallel Conversions
- General–Purpose Register for Bus–Organized Systems
- General–Purpose Registers

Absolute Maximum Ratings:

DC Supply Voltage Range (Voltages Referenced to V_{SS}), V_{DD} . . . . . −0.5 to +20V
Input Voltage Range (All Inputs) . . . . . −0.5 to V_{DD}+0.5V
DC Input Current (Any One Input) . . . . . ±10mA
Power Dissipation (Per Package), P_D
For T_A = −55° to +100°C 500mW
For T_A = +100° to +125°C . . . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation (Per Output Transistor)
For T_A = Full Package Temperature Range 100mW
Operating Temperature Range, T_A . . . . . −55° to +125°C
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +265°C

Recommended Operating Conditions: (T_A = +25°C, Note 1 unless otherwise specified)

Parameter	Symbol	V_{DD} (V)	Limits		Unit
			Min	Max	
Supply Voltage Range (Full T_A = Full Package Temperature Range)	–	–	3	18	V
Setup Time D0, D3, SR_{IN}, SL_{IN} to Clock	t_S	5 10 15	100 70 50	– – –	ns ns ns
SELECT 0, SELECT 1 to Clock		5 10 15	400 220 130	– – –	ns ns ns
Hold Time D0, D3, SR_{IN}, SL_{IN} to Clock	t_H	5 10 15	0 0 0	– – –	ns ns ns
SELECT 0, SELECT 1 to Clock		5 10 15	0 0 0	– – –	ns ns ns
Clock Pulse Width	t_W	5 10 15	180 80 50	2.0 4.0 5.5	ns ns ns
Clock Input Frequency	f_{CL}	5 10 15	– – –	3.0 6.0 8.0	Mhz Mhz MHz
Clock Input Rise or Fall Time	t_rCL, t_fCL	5 10 15	1000 100 100	– – –	µs µs µs
Reset Pulse Width	t_{WR}	5 10 15	300 200 140	– – –	ns ns ns

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the above ranges.

Static Electrical Characteristics:

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max	–	0,5	5	5	5	150	150	–	0.04	5	µA
	–	0,10	10	10	10	300	300	–	0.04	10	µA
	–	0,15	15	20	20	600	600	–	0.04	20	µA
	–	0,20	20	100	100	3000	3000	–	0.08	1000	µA
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1.0	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	mA
	1.5	0,15	15	4.2	4.0	2.8	2.4	3.4	6.8	–	mA
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	–0.64	–0.61	–0.42	–0.36	–0.51	–1.0	–	mA
	2.5	0.5	5	–2.0	–1.8	–1.3	–1.15	–1.6	–3.2	–	mA
	9.5	0,10	10	–1.6	–1.5	–1.1	–0.9	–1.3	–2.6	–	mA
	13.5	0,15	15	–4.2	–4.0	–2.8	–2.4	–3.4	–6.8	–	mA

Static Electrical Characteristics (Cont'd):

Characteristic	Conditions			Limits at Indicated Temperature (°C)							Units
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55°C	–40°C	+85°C	+125°C	+25°C			
								Min.	Typ.	Max.	
Output Voltage Low–Level V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	V
	–	0,15	15	0.05				–	0	0.05	V
Output Voltage High–Level V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	V
	–	0,10	10	9.95				9.95	10	–	V
	–	0,15	15	14.95				14.95	15	–	V
Input Voltage Low–Level V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3.0				–	–	3.0	V
	1.5,13.5	–	15	4.0				–	–	4.0	V
Input Voltage High–Level V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	V
	1.9	–	10	7.0				7.0	–	–	V
	1.5,13.5	–	15	11.0				11.0	–	–	V
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1.0	±1.0	–	$\pm10^{-5}$	±0.1	µA
3–State Output Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm10^{-4}$	±0.4	µA

Dynamic Electrical Characteristics:

(T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Operation						
Propagation Delay Time Clock to Q	t_{PHL} or t_{PLH}	V_{DD} = 5V	–	220	440	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	70	140	ns
Output Transition Time	t_{THL}, t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Minimum Setup Time: D0, D3, SR_{IN}, L_{IN} to Clock	t_s	V_{DD} = 5V	–	80	160	ns
		V_{DD} = 10V	–	35	70	ns
		V_{DD} = 15V	–	20	50	ns
SELECT 0, SELECT 1 to Clock		V_{DD} = 5V	–	200	400	ns
		V_{DD} = 10V	–	110	220	ns
		V_{DD} = 15V	–	65	130	ns
Minimum Hold Time: D0, D3, SR_{IN}, L_{IN} to Clock	t_H	V_{DD} = 5V	–	–65	0	ns
		V_{DD} = 10V	–	–25	0	ns
		V_{DD} = 15V	–	–15	0	ns
SELECT 0, SELECT 1 to Clock		V_{DD} = 5V	–	–170	0	ns
		V_{DD} = 10V	–	–95	0	ns
		V_{DD} = 15V	–	–55	0	ns

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, C_L = 50pF, R_L = 200kΩ, t_r and t_f = 20ns unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Clock Pulse Width	t_W	V_{DD} = 5V	90	180	–	ns
		V_{DD} = 10V	40	80	–	ns
		V_{DD} = 15V	25	50	–	ns
Maximum Clock Input Frequency	f_{CL}	V_{DD} = 5V	3.0	6.0	–	MHz
		V_{DD} = 10V	6.0	12.0	–	MHz
		V_{DD} = 15V	8.0	15.0	–	MHz
Maximum Clock Rise or Fall Time	t_rCL, t_fCL	V_{DD} = 5V	–	–	1000	µs
		V_{DD} = 10V	–	–	100	µs
		V_{DD} = 15V	–	–	100	µs
Minimum Reset Pulse Width	t_{WR}	V_{DD} = 5V	–	150	300	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	70	140	ns
Reset Propagation Delay	t_{PRHL}	V_{DD} = 5V	–	230	460	ns
		V_{DD} = 10V	–	90	180	ns
		V_{DD} = 15V	–	65	130	ns
Input Capacitance	C_{IN}	Any Input	–	5.0	7.5	pF

Control Truth Table

CLOCK	Mode Select S_0	Mode Select S_1	$\overline{\text{RESET}}$	Action
X	0	0	1	No Change
⎍	1	0	1	Shift Right (Q0 toward Q3)
⎍	0	1	1	Shift Left (Q3 toward Q0)
⎍	1	1	1	Parallel Load
X	X	X	0	Reset

1 = High Level
0 = Low Level
X = Don't Care

Pin Connection Diagram