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NTE4009
Integrated Circuit
CMOS, Hex Buffer/Converter (Inverting)

Description:

The NTE4009 is a hex inverter/buffer in a 16–Lead DIP type package constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. This device finds primary use where low power dissipation and/or high noise immunity is desired. The NTE4009 can be used as a current “sink” or “source” driver, CMOS–to–CMOS or CMOS–to bipolar (TTL or DTL) logic level converter, or as a multiplexer (1–to–6).

Features:

- Quiescent Power Dissipation: 50nW/package Typ
- High Current Sinking Capability: 8.0mA Min @ V_{OL} = 0.5V and V_{DD} = 10V
- Supply Voltage Range: 3Vdc to 18Vdc
- Wide CMOS–to–Bipolar Conversion Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Pin8, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD}
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics:

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage “0” Level	V_{OL}	5.0	–	0.01	–	0	0.01	–	0.05	Vdc
$V_{in} = V_{DD}$		10	–	0.01	–	0	0.01	–	0.05	Vdc
		15	–	–	–	0	–	–	–	Vdc
“1” Level	V_{OH}	5.0	4.99	–	4.99	5.0	–	4.95	–	Vdc
$V_{in} = 0$		10	9.99	–	9.99	10	–	9.95	–	Vdc
		15	–	–	–	15	–	–	–	Vdc
Noise Immunity (Note 2)	V_{NL}									
($V_{out} \geq 3.5$Vdc)		5.0	1.0	–	1.0	2.0	–	0.9	–	Vdc
($V_{out} \geq 7.0$Vdc)		10	2.0	–	2.0	3.0	–	1.2	–	Vdc
($V_{out} \geq 10.5$Vdc)		15	–	–	–	4.5	–	–	–	Vdc
	V_{NH}									
($V_{out} \leq 1.5$Vdc)		5.0	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	Vdc
($V_{out} \leq 4.5$Vdc)		15	11.0	–	–	6.75	–	–	–	Vdc
Output Drive Current Source	I_{OH}									
($V_{OH} = 2.5$Vdc)		5.0	−1.85	–	−1.25	−1.75	–	−0.9	–	mAdc
($V_{OH} = 9.5$Vdc)		10	−0.9	–	−0.6	−0.8	–	−0.4	–	mAdc
($V_{OH} = 13.5$Vdc)		15	–	–	–	−5.0	–	–	–	mAdc
Sink	I_{OL}									
($V_{OL} = 0.4$Vdc)		5.0	3.75	–	3.0	4.0	–	2.1	–	mAdc
($V_{OL} = 0.5$Vdc)		10	10	–	8.0	10	–	5.6	–	mAdc
($V_{OL} = 1.5$Vdc)		15	–	–	–	35	–	–	–	mAdc
Input Current	I_{in}	–	–	–	–	10	–	–	–	pAdc
Input Capacitance ($V_{IN} = 0$)	C_{in}	–	–	–	–	10	–	–	–	pF
Quiescent Dissipation	P_D	5.0	–	1.5	–	0.05	1.5	–	100	μW
		10	–	5.0	–	0.01	5.0	–	300	μW
		15	–	–	–	0.15	–	–	–	μW

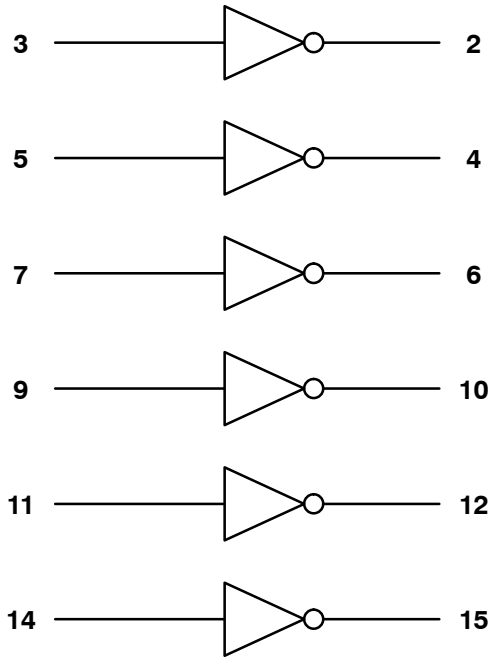
Note 2. DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal “1” or “0” input level before producing an output state change.

Switching Characteristics: (C_L = 15pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_r					
t_r = (12.4ns/pf) C_L + 44ns		5.0	–	80	125	ns
t_r = (1.0ns/pf) C_L + 20ns		10	–	35	100	ns
t_r = (0.62ns/pf) C_L + 20ns		15	–	30	–	ns
Output Fall Time	t_f					
t_f = (0.22ns/pf) C_L + 9.0ns		5.0	–	13	45	ns
t_f = (0.10ns/pf) C_L + 7.0ns		10	–	9.0	40	ns
t_f = (0.07ns/pf) C_L + 5.0ns		15	–	7.0	–	ns
Turn−On Delay Time	t_{PHL}					
t_{PHL} = (0.16ns/pf) C_L + 12ns		5.0	–	15	55	ns
t_{PHL} = (0.10ns/pf) C_L + 8.0ns		10	–	9.0	30	ns
t_{PHL} = (0.08ns/pf) C_L + 6.0ns		15	–	7.0	–	ns
t_{PHL} = (0.05ns/pf) C_L + 7.0ns		10	–	8.0	25	ns
t_{PHL} = (0.03ns/pf) C_L + 5.0ns		15	–	5.0	–	ns
Turn−Off Delay Time	t_{PLH}					
t_{PLH} = (1.0ns/pf) C_L + 35ns		5.0	–	50	80	ns
t_{PLH} = (0.40ns/pf) C_L + 19ns		10	–	25	55	ns
t_{PLH} = (0.34ns/pf) C_L + 15ns		15	–	20	–	ns
t_{PLH} = (0.36ns/pf) C_L + 20ns		10	–	25	30	ns
t_{PLH} = (0.16ns/pf) C_L + 18ns		15	–	20	–	ns

Note 3. The formulas given are for the typical characteristics only.

Logic Diagram



V_{DD} = Pin16
V_{SS} = Pin8
V_{CC} = Pin1

Pin Connection Diagram