ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE2164
Integrated Circuit
65,536 X 1 Bit Dynamic Random Access Memory
16–Lead DIP Type Package

Description:

The NTE2164 is 65,536 words by 1 bit MOS random access memory circuit fabricated with a double–poly N–channel silicon gate process for high performance and high functional density. This device uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the NTE2164 to be packaged in a standard 16–Lead DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize “false triggering” of the input, on–chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The NTE2164 also incorporates several flexible timing/operating modes.

In addition to the usual read, write, and read–modify–write cycles, th NTE2164 is capable of delayed write cycles, page–mode operation and $\overline{\text{RAS}}$–only refresh.

Proper control of the clock inputs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

Features:

- 150ns Access Time, 270ns Cycle Time
- Single Power Supply of +5V ±10% with Built–In V_{BB} Generator
- Low Power: 330mW (Active), 20mW (Standby) Max
- TTL Compatible Inputs, Low Capacitance, and Protected Against Static Charge
- Output Data Controlled by $\overline{\text{CAS}}$ and Unlatched at End of Cycle to Allow Two Dimensional Chip Selection and Extended Page Boundary
- Common I/O Capability using “Early Write” Operation
- Read–Write–Modify, $\overline{\text{RAS}}$–Only Refresh, and Page–Mode Capability
- 128 Refresh Cycle
- CAS Controlled Output Allows Hidden Refresh

Absolute Maximum Ratings:

Voltage on Any Pin Relative to V_{SS} . . . . . −1.0 to +7V
Short−Circuit Output Current 50mA
Power Dissipation 1W
Operating Ambient Temperature Range . . . . . 0° to +70°C
Storage Temperature Range . . . . . −65° to +150°C

Recommended DC Operating Conditions: (T_A = 0° to +70°C, Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input High Voltage	V_{IH}		2.4	–	6.5	V
Input Low Voltage	V_{IL}		−1.0	–	0.8	V

Note 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics: (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0° to +70°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Average Power Supply Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = min, Note 2, Note 3	–	–	60	mA
Power Supply Standby Current	I_{CC2}	$\overline{RAS}$ = V_{in}, D_{out} = High Impedance, Note 2	–	–	3.5	mA
Average Power Supply Current, Refresh Mode	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{in}, t_{RC} = min, Note 2, Note 3	–	–	45	mA
Average Power Supply Current, Page−Mode Operation	I_{CC4}	$\overline{RAS}$ = V_{in}, $\overline{CAS}$ Cycling; t_{PC} = min, Note 2, Note 3	–	–	15	mA
Input Leakage Current	I_{LI}	V_{in} = 0 to +6.5V, All other pins not under test = 0V	−10	–	+10	μA
Output Leakage Current	I_{LO}	D_{out} is disabled, V_{out} = 0 to +5.5V, Note 4	−10	–	+10	μA
Output High (Logic 1) Voltage	V_{OH}	I_{out} = −5mA	2.4	–	V_{CC}	V
Output Low (Logic 0) Voltage	V_{OL}	I_{out} = 4.2mA	0	–	0.4	V

Note 2. I_{CC} depends on output loading condition when the device is selected. I_{CC}max is specified at the output open condition.
Note 3. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.
Note 4. I_{LO} consists of leakage current only.

AC Electrical Characteristics:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance (A_0 to A_7, D_{in})	C_{in1}	Note 5	–	–	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{in2}	Note 5	–	–	10	pF
Output Capacitance (D_{out})	C_{out}	Note 5, Note 6	–	–	7	pF

Electrical Characteristics and Recommended AC Operating Conditions: (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0° to +70°C, Note 7, Note 8)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Random Read or Write Cycle Time	t_{RC}		270	–	–	ns
Read–Write Cycle Time	t_{RWC}		270	–	–	ns
Page Mode Cycle Time	t_{PC}		170	–	–	ns
Access Time from $\overline{RAS}$	t_{RAC}	Note 10, Note 12	–	–	150	ns
Access Time from $\overline{CAS}$	t_{CAC}	Note 11, Note 12	–	–	100	ns
Output Buffer Turn–Off Delay	t_{OFF}	Note 13	0	–	40	ns
Transition Time (Rise and Fall)	t_T	Note 9	3	–	35	ns
$\overline{RAS}$ Precharge Time	t_{RP}		100	–	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}		150	–	1000	ns
$\overline{RAS}$ Hold Time	t_{RSH}		100	–	–	ns
$\overline{CAS}$ Pulse Width	t_{CAS}		100	–	–	ns
$\overline{CAS}$ Hold Time	t_{CSH}		150	–	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	Note 14	20	–	50	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}		–20	–	–	ns
Row Address Set–Up Time	t_{ASR}		0	–	–	ns
Row Address Hold Time	t_{RAH}		20	–	–	ns
Column Address Set–Up Time	t_{ASC}		–10	–	–	ns
Column Address Hold Time	t_{CAN}		45	–	–	ns
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}		95	–	–	ns
Read Command Set–Up Time	t_{RCS}		0	–	–	ns
Read Command Hold Time	t_{RCH}		0	–	–	ns
Write Command Hold Time	t_{WCH}		45	–	–	ns
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}		95	–	–	ns
Write Command Pulse Width	t_{WP}		45	–	–	ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}		45	–	–	ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}		45	–	–	ns
Data–In Set–Up Time	t_{DS}	Note 15	0	–	–	ns
Data–In Hold Time	t_{DH}	Note 15	45	–	–	ns
Data–In Hold Time referenced to $\overline{RAS}$	t_{DHR}		95	–	–	ns
$\overline{CAS}$ Precharge Time (for Page–Mode Cycle Only)	t_{CP}		60	–	–	ns
Refresh Period	t_{REF}		–	–	2	ns
Write Command Set–Up Time	t_{WCS}	Note 16	–20	–	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	Note 16	60	–	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	Note 16	110	–	–	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{PRC}		0	–	–	ns

Note 7. AC measurements assume t_T = 5ns.

Note 8. 8 cycles are required after power–on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Note 9. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IH} and V_{IL}.

Note 10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the values shown.

Note 11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

Note 12. Measured with a load equivalent to 2TTL loads and 100pF.

Note 13. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Notes (Cont'd):

Note 14. Operation with the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

Note 15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read−modify−write cycles.

Note 16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above conditions are met the conditions of the data out (at access time) is indeterminate.

Pin Connection Diagram