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NTE2147
Integrated Circuit
4K Static Random Access Memory (SRAM)

Description:

The NTE2147 is a 4096–bit static Random Access Memory (SRAM) in an 18–Lead DIP type package organized as 4096 words by 1–bit. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease–of–use features associated with non–clocked static memories and the reduced standby power dissipation associated with clocked static memories. The result is low standby power dissipation without the need for clocks, address setup, and hold times. In addition, data rates are not reduced due to cycle times that are longer than access times.

$\overline{CS}$ controls the power down feature. In less than a cycle time after $\overline{CS}$ goes high – deselecting the NTE2147 – the part automatically reduces its power requirements and remains in this lower power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The NTE2147 is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non–destructively and has the same polarity as the input data. A data input and a separate three–state output are used.

Features:

- Scaled NMOS Technology
- Maximum Access Time: 55ns (Supply Current, Active: 160mA; Standby: 20mA)
- Completely Static Memory – No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power–Down
- Directly TTL Compatible – All Inputs and Outputs
- Separate Data Input and Output
- Three–State Output

Absolute Maximum Ratings: (T_A = +25°C, Note 1 unless otherwise specified)

Voltate On Any Pin (With Respect to GND), V_{IN} . . . . . –3.5V to +7.0V
DC Output Current, I_O 20mA
Power Dissipation, P_D 1.2W
Operating Temperature Range, T_{opr} . . . . . –10° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not inplied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics: (T_A = 0° to +70°C, V_{CC} = +5V ±10%, unless otherwise specified, Note 2 & 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Load Current (All Input Pins)	I_{LI}	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	0.01	10.0	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}	–	0.01	10.0	µA
Operating Current	I_{CC}	T_A = +25°C, V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open	–	120	150	mA
		T_A = 0°C, V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open	–	–	160	mA
Standby Current	I_{SB}	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}	–	12	20	mA
Peak Power–On Current	I_{PO}	V_{CC} = GND to V_{CC} = Min, $\overline{CS}$ = Lower of V_{CC} or V_{IH}Min, Note 4	–	25	50	mA
Input Low Voltage	V_{IL}		–3.0	–	+0.8	V
Input High Voltage	V_{IH}		2.0	–	6.0	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	–	–	V
Output Short Circuit Current	I_{OS}	V_{OUT} = GND to V_{CC}	–150	–	+150	mA

Note 2. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 3. Typical limits are V_{CC} = 5V, T_A = +25°C and specified loading.

Note 4. I_{CC} exceeds I_{SB} maximum during power on. A pull–up resistor to V_{CC} on the CS input is required to keep the device deselected: otherwise, power–on current approaches I_{CC} active.

Capacitance: (T_A = +25°C, f = 1MHz, Note 5 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	6	pF

Note 5. This parameter is sampled and not 100% tested.

AC Test Conditions:

Input Pulse Levels . . . . . GND to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V

AC Characteristics: (T_A = 0° to +70°C, V_{CC} = +5V ±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read Cycle						
Read Cycle Time	t_{RC}	Note 6	55	–	–	ns
Address Access Time	t_{AA}		–	–	55	ns
Chip Select Access Time	t_{ACS1}		–	–	55	ns
	t_{ACS2}		–	–	55	ns
Output Hold from Address Change	t_{OH}		5	–	–	ns
Chip Select to Output in Low Z	t_{CZ}	Note 7, Note 8	10	–	–	ns
Chip Deselection to Output in High Z	t_{HZ}	Note 7, Note 9	0	–	30	ns
Chip Selection to Power–Up Time	t_{PU}		0	–	–	ns
Chip Selection to Power–Down Time	t_{PD}		–	–	20	ns

Note 6. All Read Cycle timings are referenced from the last valid address to the first transitioning address.

Note 7. At any given temperature and voltage condition, t_{HZ}max is less than t_{LZ}min both for a given device and from device to device.

Note 8. Transition is measured ±200mV from steady state voltage with specified loading.

Note 9. Transition is measured at V_{OL} +200mV and V_{OH} –200mV with specified loading.

AC Characteristics (Cont'd): (T_A = 0° to +70°C, V_{CC} = +5V ±10%, unless otherwise specified)

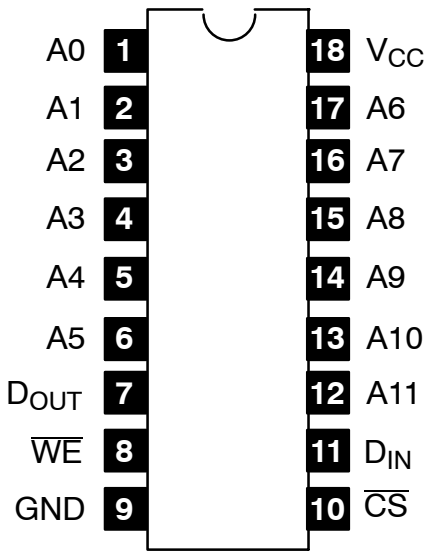
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Write Cycle						
Write Cycle Time	t_{WC}	Note 7	55	–	–	ns
Chip Select to End of Write	t_{CW}		45	–	–	ns
Address Valid to End of Write	t_{AW}		45	–	–	ns
Address Setup Time	t_{AS}		0	–	–	ns
Write Pulse Width	t_{WP}		25	–	–	ns
Write Recovery Time	t_{WR}		10	–	–	ns
Data Valid to End of Write	t_{DW}		25	–	–	ns
Data Hold Time	t_{DH}		10	–	–	ns
Write Enable to Output with Z	t_{WZ}	Note 8	0	–	25	ns
Output Active from End of Write	t_{OW}	Note 9	0	–	–	ns

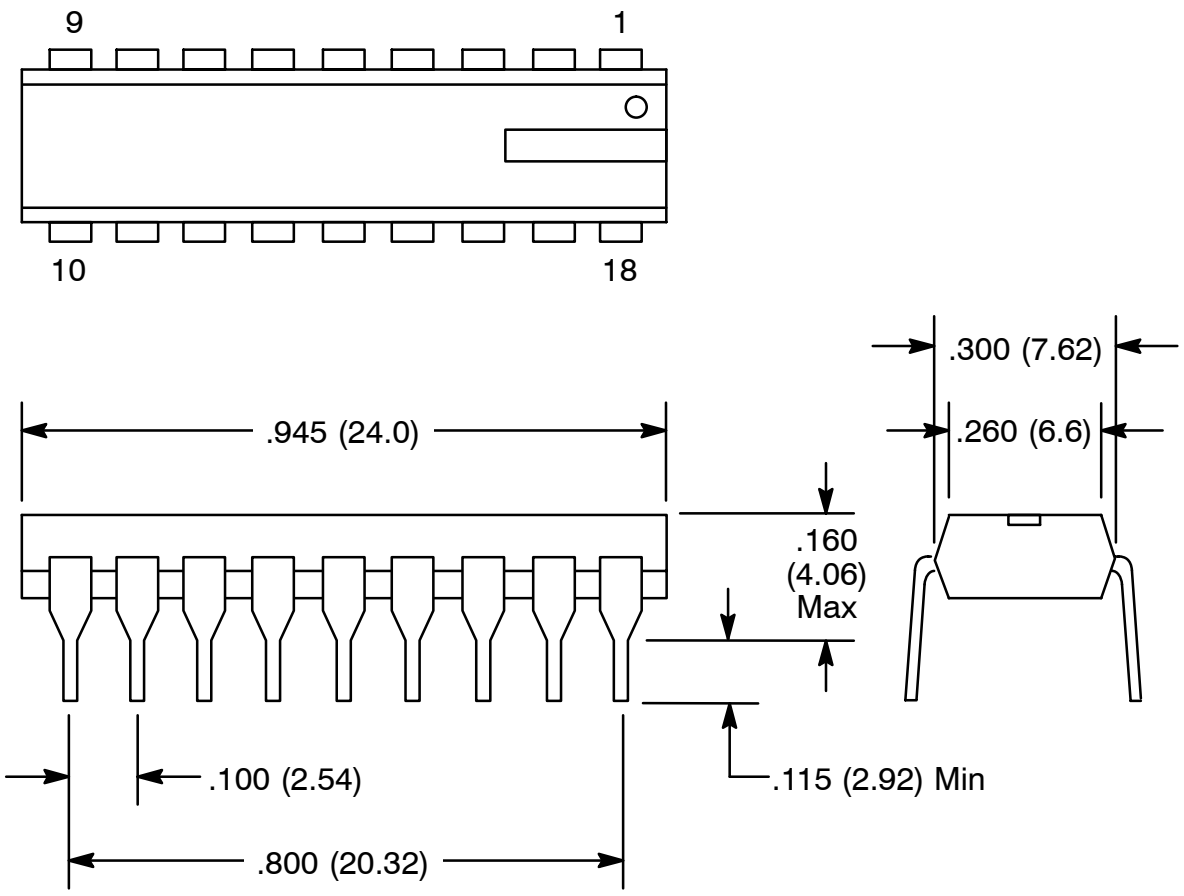
Note 7. At any given temperature and voltage condition, t_{HZ}max is less than t_{LZ}min both for a given device and from device to device.
Note 8. Transition is measured ±200mV from steady state voltage with specified loading.
Note 9. Transition is measured at V_{OL} +200mV and V_{OH} −200mV with specified loading.
Note 10. WE is high for Read Cycle.
Note 11. Device is continuously selected, $\overline{CS}$ = V_{IL}.
Note 12. Address valid prior to or coincident with $\overline{CS}$ transition low.

Truth Table:

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

Pin Connection Diagram




9
1
10
18
.300 (7.62)
.260 (6.6)
.945 (24.0)
.160
(4.06)
Max
.100 (2.54)
.115 (2.92) Min
.800 (20.32)